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Idaho National Lab Impedance Measurement Box High Voltage Coupling Circuit

Mark Clagett
Montana Tech of the University of Montana

Andrew Storro
Montana Tech of the University of Montana

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Idaho National Lab Impedance Measurement Box High Voltage Coupling Circuit

Mark Clagett & Andrew Storro

Mentor(s): John Morrison & Jon Christophersen

Montana Tech

2014-2015

Introduction

Our project goal is to build a 300V [1] coupling circuit for the Idaho National Lab's (INL) Impedance Measurement Box (IMB). The IMB is a device that determines the frequency spectrum of the internal impedance of a battery by measuring its impedance to various frequencies. The procedure involves the box outputting a sum of sines (SOS) signal into a battery, capturing its voltage response, and processing the voltage time record into an impedance spectrum. This allows the box to determine the internal impedance of the battery, which can be used to predict the battery's life and other characteristics. [2]

The IMB is currently built to measure batteries of up to 50V. Our goal is to design and construct a circuit that will allow the box to measure batteries of up to 300V. This will be done through the use of a coupling circuit and a state machine. The coupling circuit will operate by using a high voltage capacitor and resistors to protect the IMB and allow it to measure the battery without the source voltage ever exceeding 30V, which is the max the future IMB is designed to safely handle.

Our deliverables at the end of the spring semester include:

- Working prototype of the system with a design goal of working with batteries of up to 300V.
- Complete design documentation with test results.
- A final report that documents the function and operation of the system.
- A final presentation and Texpo poster.

There are also several key requirements and constraints we kept in mind while designing this circuit.

Requirements:

- The IMB will be able to safely and accurately measure the impedances of batteries up to 300V.
- The IMB current source not actively be exposed to any voltages above 30V.
- A working prototype of the circuit and state-machine will be constructed.

Time Constraints

- Order all components needed within the first week back from winter break.
- Have a working model of the state-machine operational within the first two-three weeks back from winter break.
- Build a full circuit that can run the IMB within a week of the components arriving.
- Design and order a PCB after successfully testing the circuit.
- By mid-March have the full system working.
- Rough draft of the final report prior to spring break.
- Prepare for the Texpo /Symposium starting after spring break.

Part 1: Simulation and Design

Analytical Validation

In order to explore the possibility of this project, an analytical validation was performed to ensure that the concept was feasible. In order to do this we configured a Matlab model of the measurement concept. A preliminary design for the coupling circuit is shown in Figure 1, this was used to develop the Matlab model.

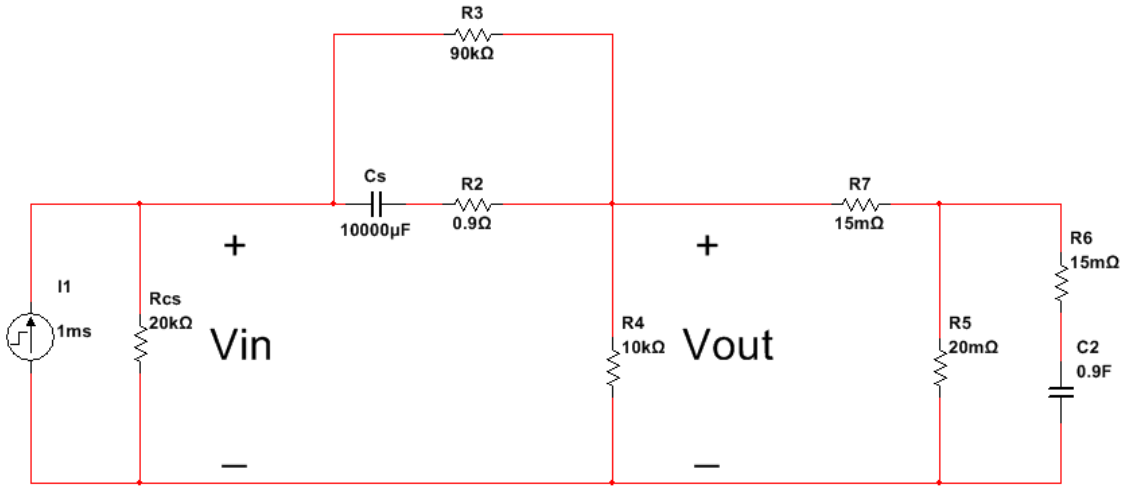


Figure 1: Preliminary Coupling Circuit Design

This circuit is rather complicated and bears further explanation. Starting with the right side of the circuit, Figure 2, the test cell, a circuit that has impedance comparable to a test battery. [3]

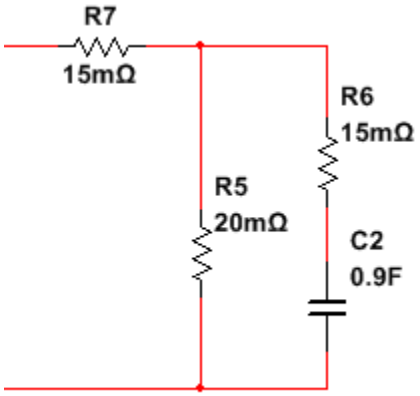


Figure 2: Test Cell

This part of the circuit simulates the internal components of the battery itself. Using this as a base model we can simulate a batteries response to various input frequencies.

Figure 3 illustrates the equivalent circuit of the coupling capacitor. [4] Where Cs is the capacitor, R2 models the leakage resistance and R3 models the series resistance. These are typical values given in the vender data.

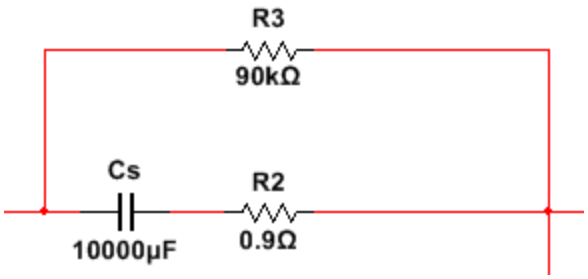


Figure 3: Coupling Capacitor

The coupling capacitors primary goal is to block the IMB current drivers from high voltages. This means that the voltage over the current source must not exceed 30V. When a test is initiated the capacitor should charge to about 300V, or whatever the batteries voltage is, thus keeping the voltage over the current source very low.

The whole circuit works as follows. A battery is connected to the circuit, in this case our test cell. The capacitor is charged by the battery voltage until the voltage that would be seen by the IMB is negligible. The IMB current source is then connected to the circuit and conducts the test.

The simulation was to prove the circuit actually works as described. Using the circuit shown in Figure 1, we defined numerous constants which simplified the transfer function. These constants, which are listed in the attached code, were used to build the recursive model. Our final transfer function is shown below.

$$\frac{Vout(\$)}{Vin(\$)} = \frac{Ztc}{Ztc+Zcc+Rcs} \tag{1}$$

Where:

$$Ztc = \frac{\left(Rs+*R3*\left(R2+\frac{1}{\$*C1}\right)+Rs*R1*\left(R3+R2+\frac{1}{\$*C1}\right)\right)}{(Rs+R1)*\left(R2+R3+\frac{1}{\$*C1}\right)+R3*\left(R2+\frac{1}{\$*C1}\right)} \tag{2}$$

$$Zcc = \frac{Rlk*\left(Resr+\frac{1}{\$*Cs}\right)}{Rlk+Resr+\frac{1}{\$*Cs}} \tag{3}$$

$$Vin = Iin * Rcs \tag{4}$$

Vin is the voltage over the current source, Ztc is the test cell impedance, Zcc is the coupling capacitor impedance, and Vout is the voltage over the test cell.

Once we had the transfer function our next step was to simulate the circuit. We did this two ways, first with Multisim, and second with Matlab. Using Multisim we built the circuit as shown in Figure 1, and recorded the test cell's voltage response to a step input.

Then with Matlab, using the transfer function and the recursive method, we simulated and calculated the same step response. This transfer function is in the S domain, while the recursive method needed to be changed into the discrete time domain. This was done by using the equation: $\$^n = \frac{dt^n}{(z-1)^n}$, then, using the state variable method outlined in the "Book of John," [5] we found the output voltage.

The step responses were all plotted together for comparison and shown in Figure 4.

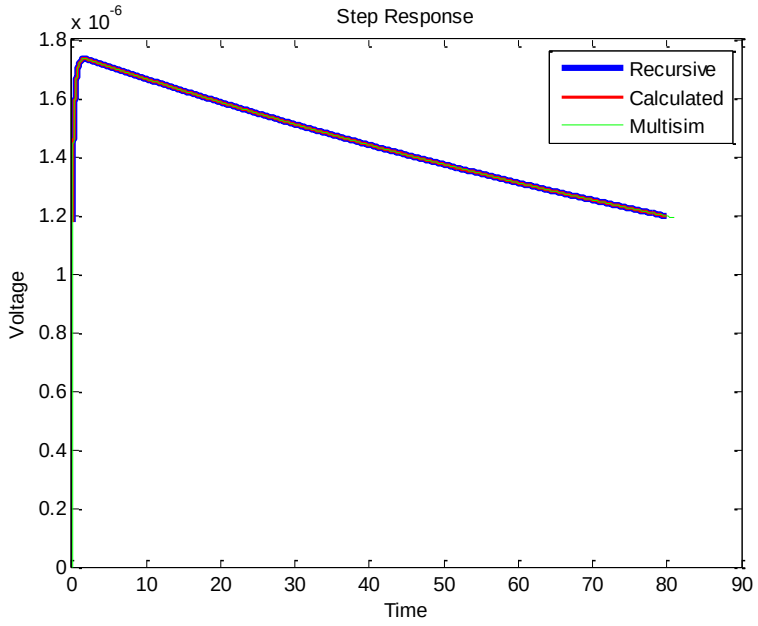


Figure 4: Step Responses for all Methods

The very close alignment between the step responses of the Multisim model and the Recursive model is analytical validation for the recursive model. That model will now be used to simulate the response of the recursive model of the coupling circuit to a simulated time recorder of the sum of sines (SOS) current used by the IMB to acquire a spectrum from the test battery. The model will predict the voltage across the IMB current source, the voltage across the coupling capacitor and the voltage across the test cell. This later will be post processed via the HCSD algorithm [6] to obtain the impedance spectrum.

The IMB uses an SOS signal of 62.5mA and ranging from 0.0125Hz-3276.8Hz to measure the impedance so that is what we will use here. The test cells current and voltage response of this signal is shown in Figure 5.

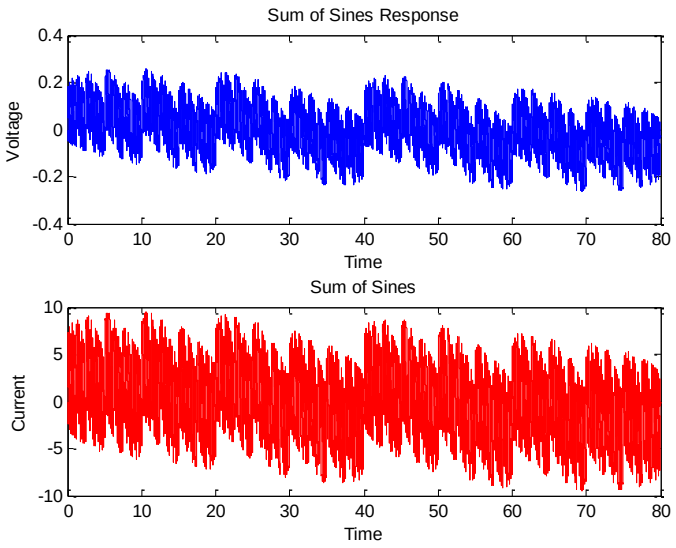


Figure 5: Sum of Sines Current and Test Cell Voltage Response

This shows that the coupling capacitor circuit will allow the SOS current to pass through it without corrupting the signal.

The simulated test cell voltage time record was processed with the IMB data processing algorithm and plotted in the Nyquist format with the theoretical test cell impedance[2].

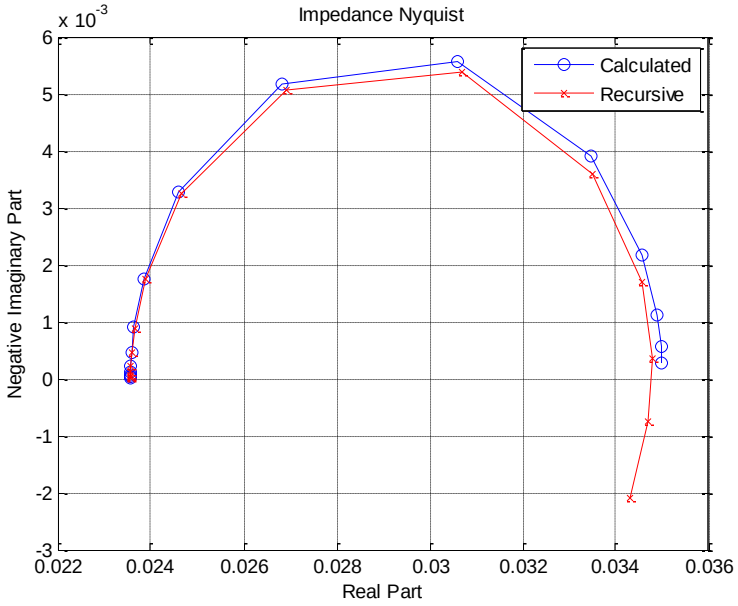


Figure 6: Nyquist Impedance Plot

This theoretical Nyquist response was found by calculating the real and imaginary impedances based on the jω analysis of the inputted frequencies. These were then plotted against each other to show how they related to one another. The plot shows that the calculated response of the system closely correlates with the recursively simulated response, providing the validity of our proposal. The calculated plot is an

entirely mathematical interpretation of the system, while the recursive is a simulation of the voltage and current inputs of the system. The code used for all these steps is shown in the Appendix.

These plots show a fairly accurate representation of what the IMB would produce if it measured a battery with these characteristics. This is an accurate analytical validation of the simulation and has allowed us to investigate what characteristics of the coupling circuit components would be.

In order to prove that the system could work safely, (manage up to 300 V) and that the box wouldn't be exposed to excessive voltages (30V), different recursive simulations were run using the same SOS current to determine the voltage across the capacitor and the voltage across the current source. These simulations produced Figures 7 and 8, respectively. When compared side-by-side the two plots are mirror images of each other. The main concern here was whether the capacitor could protect the IMB by keeping the voltage over the current source below 30V, which as shown it does.

It was at this point we began to run into issues. Due to algebra, coding errors and time constraints, we started having troubles building the recursive model. After about a month and half of work we had the correct shaped response of the current source plot, but our magnitude was off by several orders. In the end John lent us his code for simulating the voltage of the current source and capacitor in order to move on to the design.

In order to determine if the simulation would violate the system requirements, we, using John's code, simulated the voltage the capacitor would experience during a test, and the voltage that the BOX SOS current source would see. To solve for the latter, we determined the transfer function:

$$\frac{Vout}{Vin} = \frac{Rcs}{Rcs + Ztc + Zcc}$$

As shown in Figure 1, Rcs is the resistance over the current source, Ztc is the impedance of the test cell, and Zcc is the impedance of the coupling capacitor.

This transfer function simulated the voltage across Rcs, since Rcs is in parallel with the source, finding the voltage drop over Rcs produces the same result. Once the source voltage was known, we could calculate the voltage across the capacitor by taking the voltage of the battery and subtracting the current source voltage from it. This works because the battery voltage is a constant 300V and the current source varies in response to the SOS current, therefore, any difference between the two is seen by the capacitor. Figures (7)&(8) show the voltage response across these components. Assuming a 300V battery voltage and the same SOS current used in the impedance measurement.

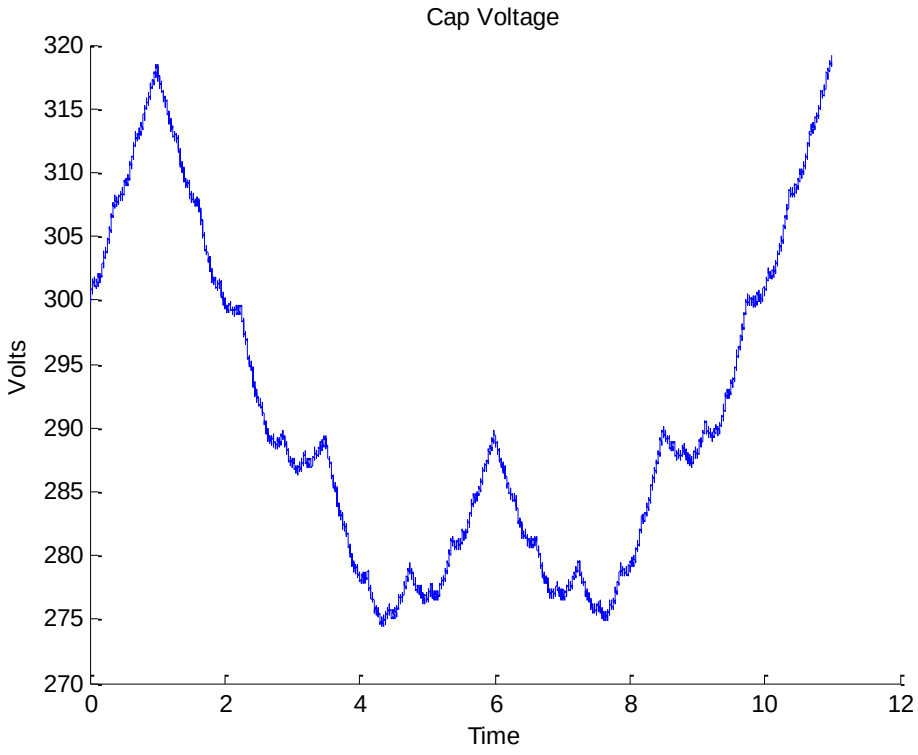


Figure 7:Voltage over the Capacitor

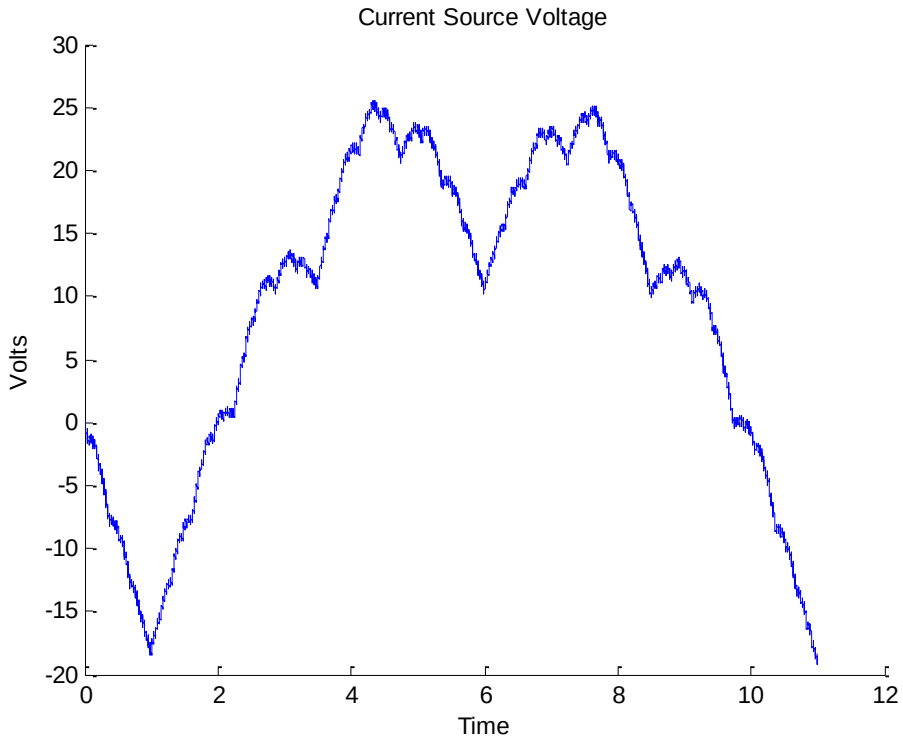


Figure 8: Voltage over the Current Source

As Figure 7 shows the voltage response across the coupling capacitor (Cs from Figure 1), provided that the capacitor is valued at 0.01F and has a voltage rating greater than or equal to 320V (vender data gives it as 450V)[3] the system will be able to handle a 300V test cell. Figure 8 on the other hand displays the estimated voltage the IMB current source will see while making its measurement, as previously stated this voltage cannot exceed 30V or damage to it will occur, the simulation shows that the voltage will be approximately 25.5V which is within the given parameters.

The code used for all these simulations is given in the Appendix.

Part 2: Physical Validation

Coupling Circuit Design Description

The establishment of analytical validation was followed with a physical validation. With design and development of the coupling circuit and control. Which will lead to the final effort of testing that establishes physical validation.

Figure 9 illustrates the concept for the coupling circuit.

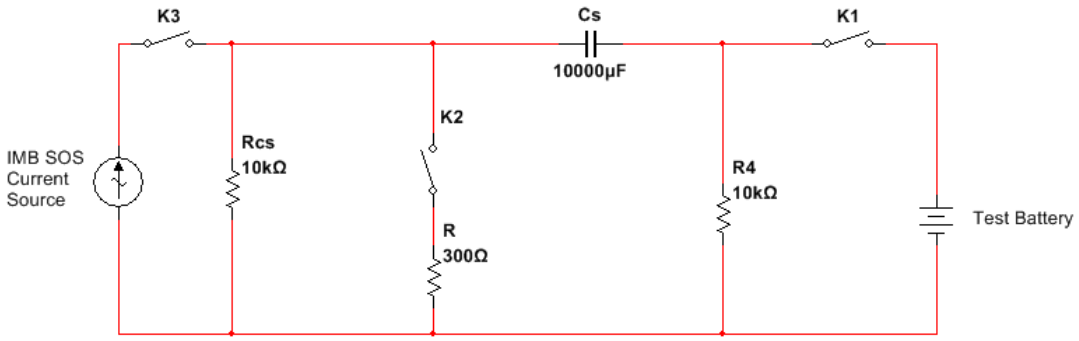


Figure 9: Overview of Coupling Circuit w/ Control Switches

The circuit functions as follows using relays K1, K2 and K3 to control the system. A user input initiates a test, closing K1 and K2. This allows the coupling capacitor to charge to a voltage equal to that of the battery. The voltage over the 300 Ω resistor(R) is monitored to determine when the capacitor is fully charged. While the voltage over R is greater than 30V, K3 will never open thus protecting the IMB current drivers. Once the voltage over R has dropped to about 1% of the test battery's voltage, K2 will open and K3 will close, connecting the IMB to the circuit. A signal will be sent to the IMB at this point to trigger a measurement. Once the measurement has been completed all the relays open.

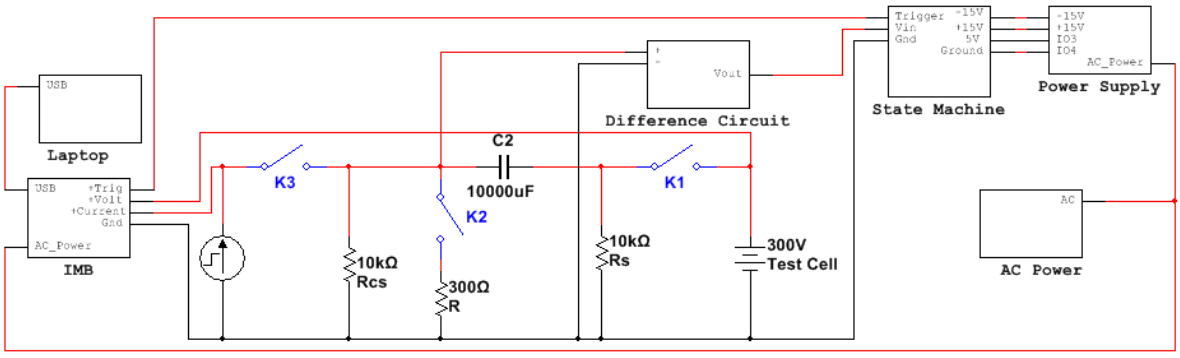


Figure 10: General Overview of Full Circuit Design

Figure 10 illustrates a general overview of the full design. The IMB is connected to our circuit in four places: a common ground, the voltage connection for the battery, the current connection for the SOS

input, and a trigger connection from the state machine. A difference op-amp is connected over the 300 Ω resistor and outputs to the state machine. The state machine is powered by an AC/DC converter with outputs of +5V, +15V, -15V and GND. More detail on each component is given below.

The difference op-amp was designed with two comparators that would monitor the voltage over the 300Ω resistor which would tell us when the capacitor was charged or if the voltage was greater than 30V. The overall designed ended with the following operation, when the voltage over the 300Ω resistor is around 1% the voltage over the battery, the relays were allowed to close. Furthermore, if the voltage ever went to 30V or higher the K3 was forced open. The gain of the op-amp was also designed that in case of an emergency it could handle an input voltage of 300V without being damaged. The final difference op-amp and comparators circuit connected to the coupling circuit is shown below in Figure 11.

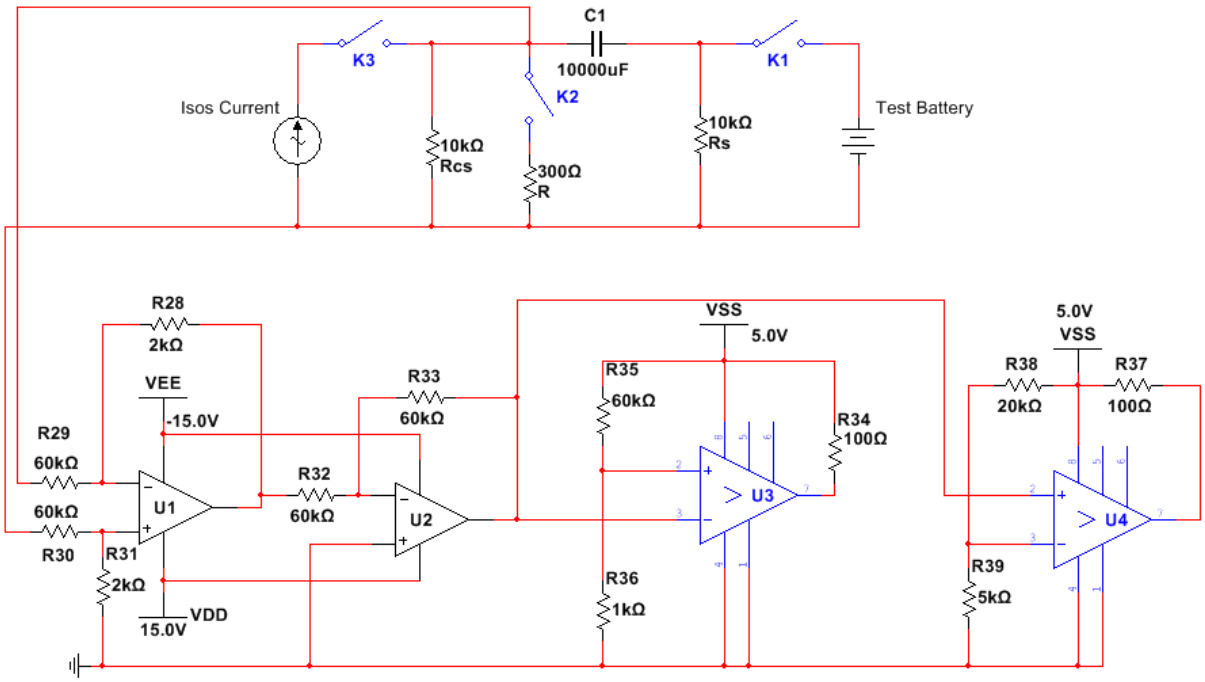


Figure 11: Interface Control Monitor for Coupling Circuit

Figure 11 illustrates the control monitoring the state of the coupling circuit. It operates as follows. The first difference op-amp (U1) works by reading in two different voltages and outputting the difference between the two, the second one (U2) is to invert it back to a positive value. In this case it is reading the voltage over the current source. When the voltage over the 300Ω resistor is almost zero the coupling capacitor is fully charged. However, because we are designing to test a 300V battery and 741 op-amps are only rated to handle a voltage difference of 30V, based on the available power supply, the gains on the op-amp had to bring any input voltage down to a safe level. Therefore a gain of 1/30 was used to bring a max voltage of 300V down to 10V, which is all the op-amp will see. Then because the difference op-amp is technically an inverting op-amp as well it outputted a negative voltage. To fix this a simple inverting op-amp was added with a gain of 1. It should be noted here that by switching the input connections of U1 it is possible to remove U2 from the design, however this was not noted until after design had been completed and so was not implemented.

The second and third parts of this circuit are the comparators. These will take an input voltage, compare it to some other voltage and output 0V or 5V depending on the input. If the input is lower than the static voltage, the positive terminal, it outputs 5V, otherwise the output is 0V. The first comparator looks for a voltage of almost zero, which is what the difference op-amp outputs when it sees almost zero volts. The second capacitor is looking for a voltage of 1V which is what the difference op-amp outputs when it sees 30V. These comparators are what will ultimately control the relays of our state-machine.

The IMB can be programmed to look for a trigger signal input to tell it when to make a measurement. So a one-shot circuit was designed to output such a trigger to the IMB when the coupling system was ready to make a measurement. Also, all the switches need to open automatically once a measurement is done. The IMB also uses TTL logic to control its internal relays. By monitoring this signal we can use it to tell our circuit when a test has been complete and to reset all the relays.

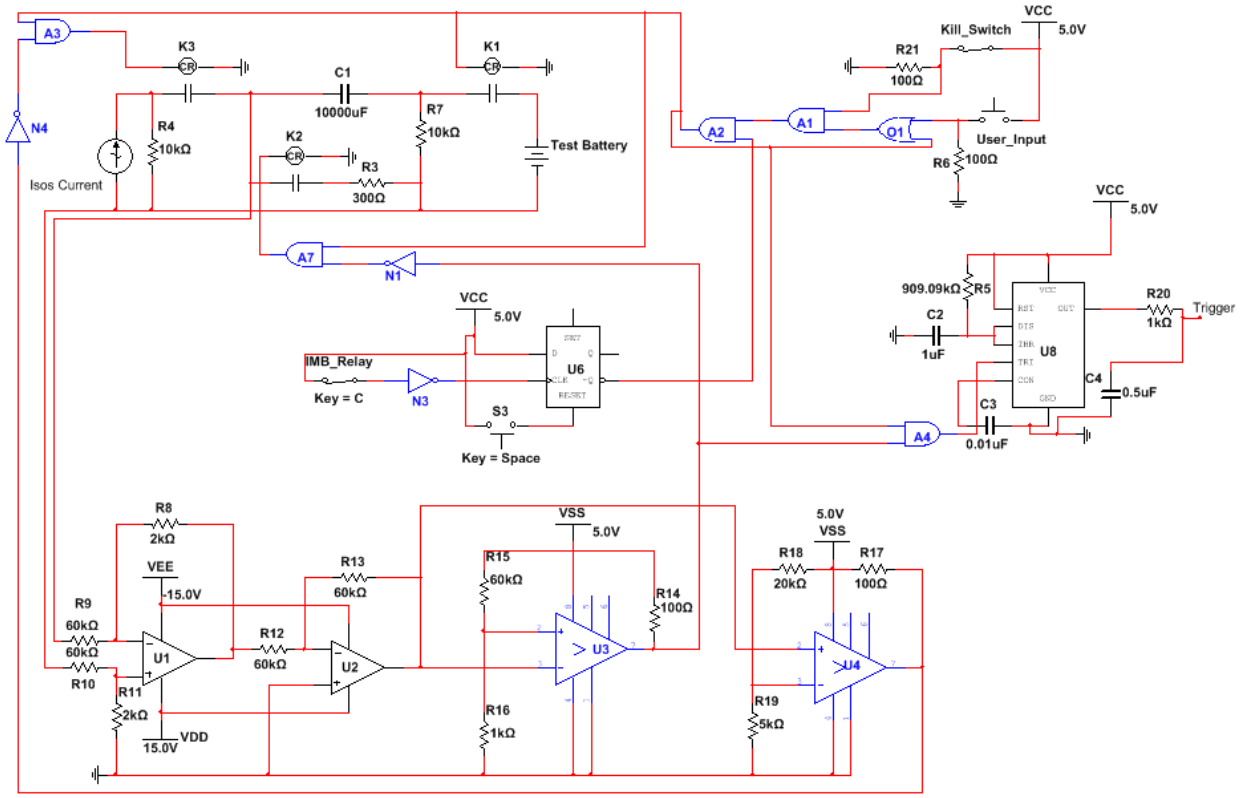


Figure 12: Final Coupling Circuit with State Machine Discharged State

Figure 12 illustrates the full system. The state machine had to meet the following requirements:

- Have a user controlled push button input that tells the system to make a measurement. (User_Input)
- Have an emergency kill switch that opens all relays.(Kill_Switch)
- Once the User_Input has been pressed, automatically charges the capacitor (C1) and when charged sends a trigger pulse to the IMB (Trigger), which begins the test sequence.
- When finished measuring the IMB relays will reopen (IMB_Relays), and the system automatically opens all relays and prepares for a new test.

- Throughout the test should the voltage over the IMB connections to the current source ever exceed 30V, all relays automatically open and end the test.

The final circuit with the entire state machine, with the relays in the non-test condition is shown in Figure 11. K1 connects the battery to the circuit, K2 charges the capacitor, and K3 connects the IMB to the circuit.

Figure 13 shows the final circuit during a measurement. The control pushbutton (User_Input) was pressed, closing K1 and K2 to charge the capacitor (C1). When C1 is charged, the difference op-amp (U1 and U2) sees a very small voltage drop and comparator 1 (U3) outputs 5V. That voltage is inversed (N1) to 0V which causes K2 to open. Comparator 2 (U4) doesn't output 5V because the voltage is less than 30V. Because a test has been initiated and U4 is outputting 0V, K3 closes. With U3 outputting 5V and K1 being closed, the 555-Timer (U8) output step up from 0V to 5V which triggers the IMB to initiate a measurement.

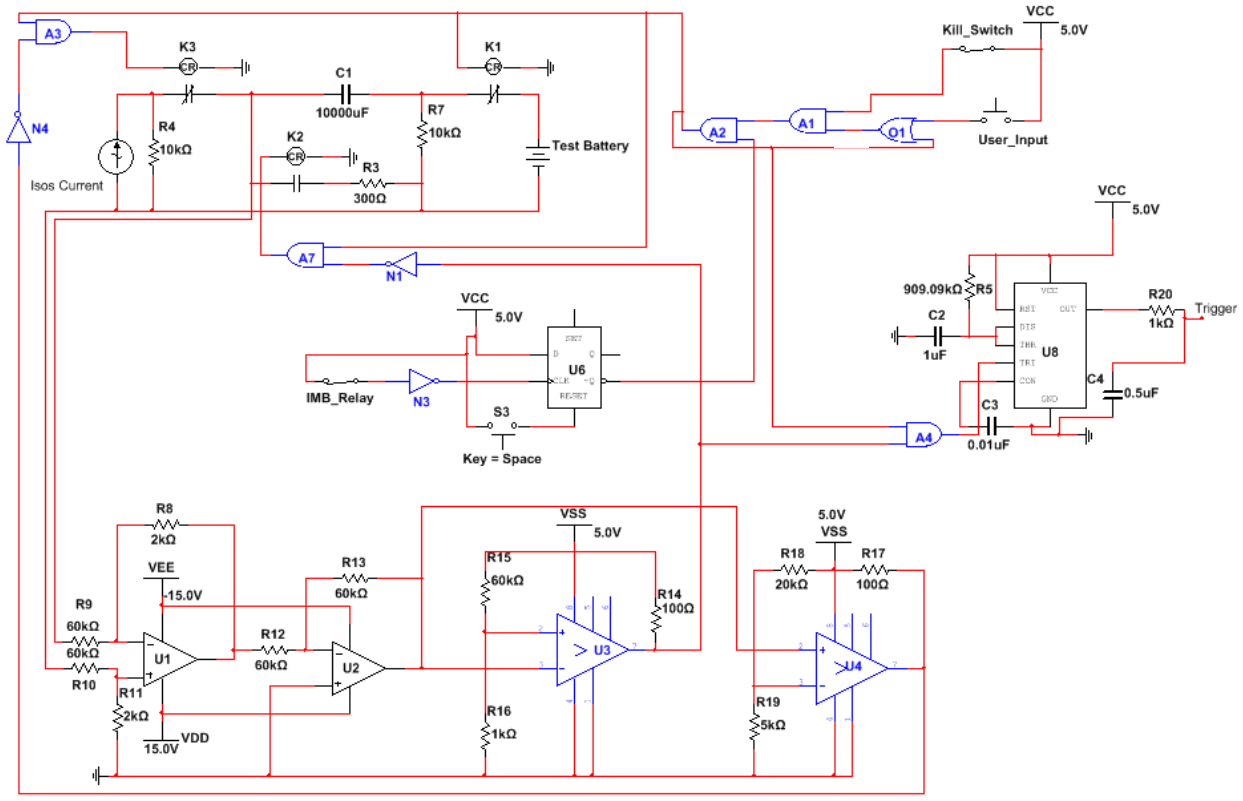


Figure 13: Final Coupling Circuit with State Machine during a measurement

An explanation is provided as to what is going on here, starting with the user controlled inputs, shown in Figure 14.

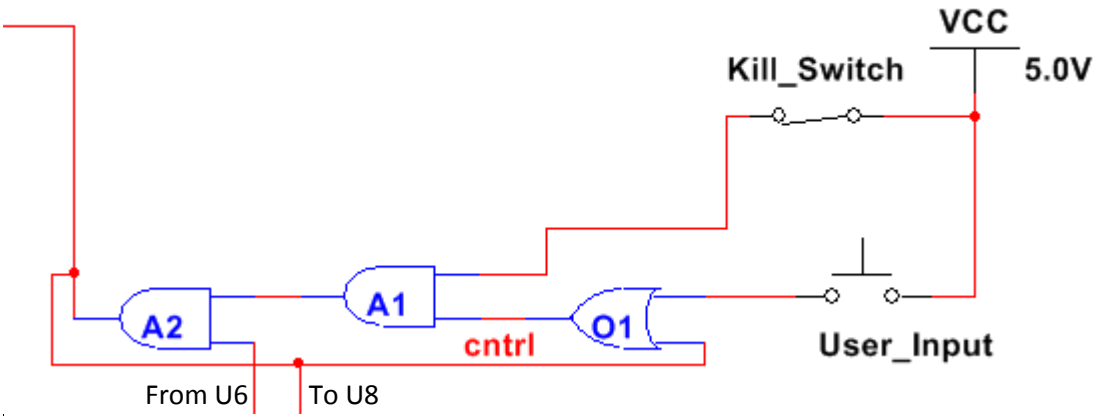


Figure 14: User Controlled Inputs

Figure 14 models both the User_Input and the Kill_Switch. The output of this portion is one of the controllers for each relay. When the User_Input is pressed it sends 5V to the O1, which is looking for 5V on any of its inputs. If it sees 5V it outputs 5V to A1, if not it outputs 0V. Once O1 has sent 5V to A1 it will see 5V on its second input until the test is ended, because the entire control portion's output is connected to the second input.

A1 takes an input from both O1 and Kill_Switch. Kill_Switch, when closed will send 5V to A1 allowing the User_Input value to pass. If Kill_Switch is open, A1 outputs 0V which will open all the relays.

A2 takes an input from A1 and the inverse output of U6. U6 is a Data Flip-Flop (DFF) whose normal output is 0V until it sees a negative edge signal from the IMB, signifying the test is done.

Once a test has been initiated, A2 will output 5V constantly until one of two things happens; either the test is finished and N2 outputs 0V to A2, or the Kill_Switch closes and outputs 0V to A1.

Next is our coupling circuit with controllers.

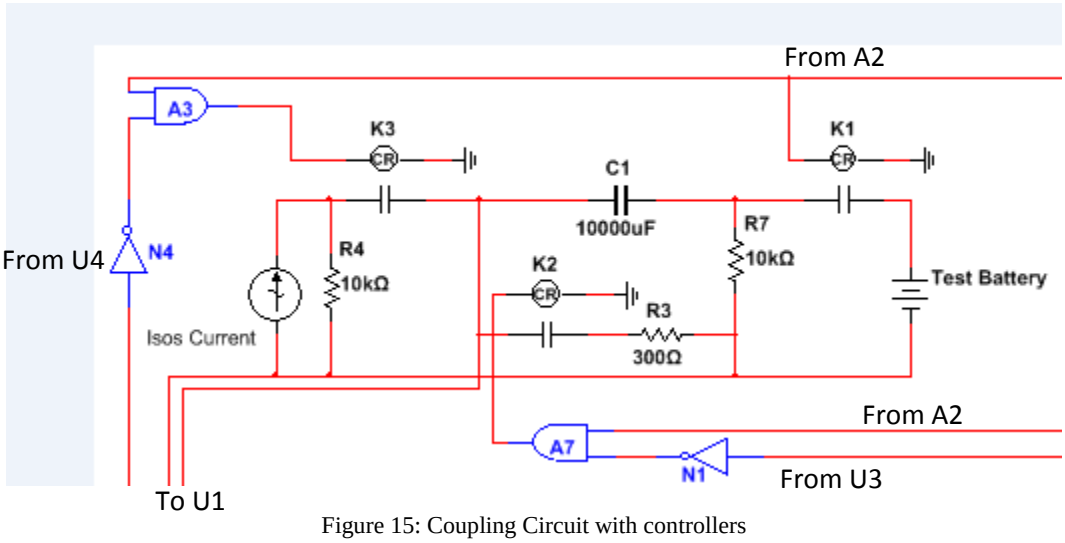


Figure 15: Coupling Circuit with controllers

This portion shows the output from A2 going to our relays. The 300V battery and is what charges C1. For this case the test cell is not included because it reflects the batteries internal components. This circuit shows the operation of the circuit during a test.

The relays are normally open and close when current is ran through their coils. As you can see, the only relay that is primarily controlled by A2 is K1. K1 is the relay that connects the battery to the circuit when the User_Input is pressed. It will only reopen if the Kill_Switch is closed or the test is done.

K2 is controlled by A7 which is in turn controlled by A2 and N1. N1 is the inverse of the signal from U3.. When the blocking capacitor is not charged, U3 outputs 0V to N1, which sends 5V to A7. This will allow the controller to close when a test is initiated. Then, once the blocking capacitor has fully charged, the comparator outputs 5V to N1. N1 sends 0V to A7 which passes that along to K2 which then reopens.

K3 is our kill switch which is controlled by A3. A3's inputs are from A2 and N4. N4 takes the signal from U4 and inverses it. In this case, U4 will only output 5V to N4 if a voltage of over 30V is detected over the 300Ω and K2. If that happens, N4 sends 0V to A3 and K3 opens, otherwise K3 will remain closed.

Next we have the difference op-amp portion.

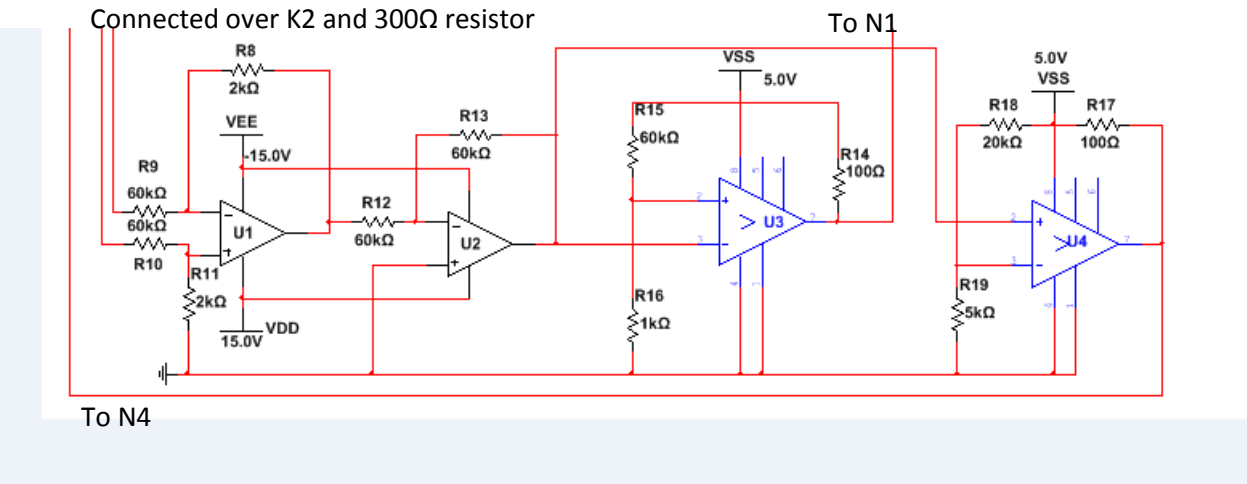


Figure 16: Difference Op-Amp and Comparators

The two inputs of U1, a 741 op-amp, are connected over the 300 Ω resistor and it outputs the voltage difference it sees with a gain of 1/30. This gain was chosen to protect the op-amps from excessively high voltages and prevents saturation or damage, the validation for this gain is outlined in Appendix D. U1 outputs an inverse voltage so U2, another 741 op-amp, inverses the difference again to create a positive voltage. U2 then outputs directly into LM311's U3 and U4. These comparators normally output 0V. When the inputs of U1 are almost 0V, U3 will output 5V, and when the inputs are greater than 30V, U4 will output 5V.

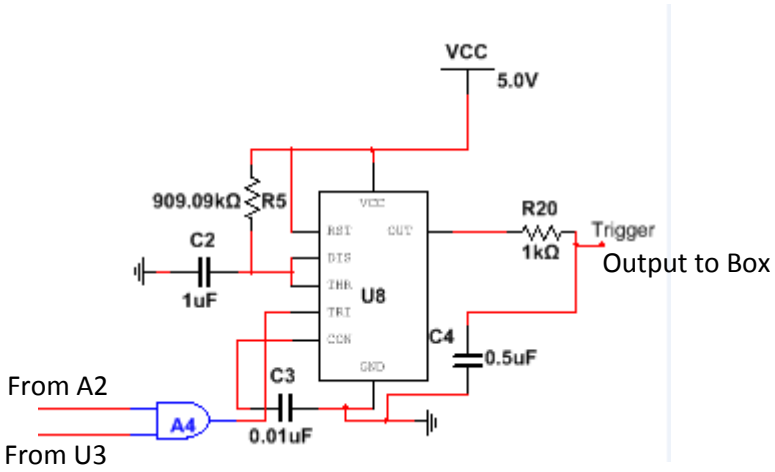


Figure 17: One-Shot Circuit

Figure 17 illustrates the trigger circuit that tell the IMB to begin the measurement. Using a 74161 (555) chip (U8) a circuit that outputted a one second pulse was designed. However, we only want it to output a when a test has been initiated, and the capacitor is charged. A4 is what controls the operation of the one shot. When it outputs 5V, the one-shot operates just one time, per test. Otherwise it remains in its current state. A4's inputs are from A2, and from U3. This is because we only want the one-shot to operate after a test has been initiated and the blocking capacitor is charged.

Due to the way the logic works there was a slight bounce on the trigger pulse so a RC de-bounce was added to the output to smooth the signal out. This was done with the 1kΩ resistor and the 0.5µF capacitor shown in Figure 17. Once the output is triggered, it will not trigger again until a new test is initiated.

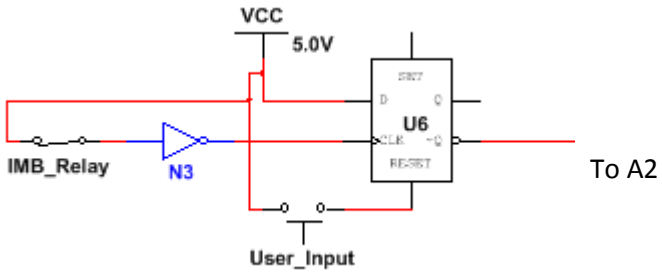


Figure 18: DFF End of Test Signal

There was no real way to simulate the internal relays of the IMB opening to signify the end of a test. Therefore, a switch was used for this (IMB_Relay). In the actual build of the circuit we will use a difference op-amp and a comparator to accomplish this. When the DFF (U6) sees the negative edge of a TTL signal, meaning the IMB has reopened its relays, the inverse output U6 will send a 0V signal to A2. This tells all the relays to reopen and allows the capacitor to discharge. Because a DFF will hold output value until it sees another TTL edge, it is tied to reset every time a test is initiated via User_Input.

In summary, when the user inputted button is pressed, controllers K1 and K2 close and the coupling capacitor begins charging. Once charged, K2 opens and K3 closes. A trigger pulse is sent to the IMB and a measurement is made. Once done, the DFF detects when the internal IMB relays re-open and opens both K1 and K3, allowing the capacitor to discharge.

Build and Testing

At the start of the spring semester we started building our full circuit for testing. There were three main components which needed to be built in order so they could be tested; the first being the difference op-amp circuit to measure the voltage over the 300Ω resistor; second, the logic to control the relays; and third, the coupling capacitor circuit. This section will highlight the building of the circuit and issues that were encountered during testing.

The difference op-amp circuit, shown in Figure 11, was built and tested by putting a varying voltage over the two input leads of U1, normally connected over the 300Ω resistor. When the voltage exceeded 30V the U4 outputted 5V, and when the voltage was almost zero the U3 outputted 5V, as designed. This portion did not receive any changes as a result of testing.

The second part we built was the logic that controlled all the relays. The logic that controlled each relay had to be changed to ensure better security and added functionality, as it was noticed during testing the current logic did not account for all situations. The User_Input and Kill_Switch had pulldown resistors added to remove floating pin errors. It was noticed that without these resistors, tests either would not initiate or initiate without user input.

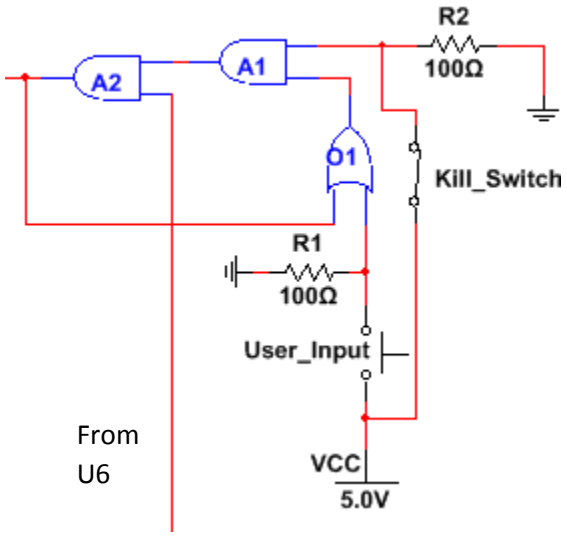


Figure 19: Control logic with pulldown resistors

The control for the K2 resistor received the most changes. Initially it was just dependent on the output of U3 and A2. It was observed that during a test, the K2 relay would open and close during a test as a result of the changing voltage over the 300Ω resistor from the SOS current from the IMB. To overcome this, a second DFF (U5) was added that would clock when K2 opened after closing once. The inverse output of U5 was added to the logic that controlled K2, which prevented it from reclosing after it had closed once. This DFF was tied to reset with User_Input.

It was also noticed during simulation, that once a test had been run, if another test was initialized immediately, the logic would never run through correctly. This was due to K2 needing to close and reopen to clock U5. To correct this, an optional discharge switch (Discharge) was added that would allow K2 to close when a test was not being run in order to discharge the capacitor quicker. During testing it was observed that by allowing thirty seconds to discharge, the logic worked correctly.

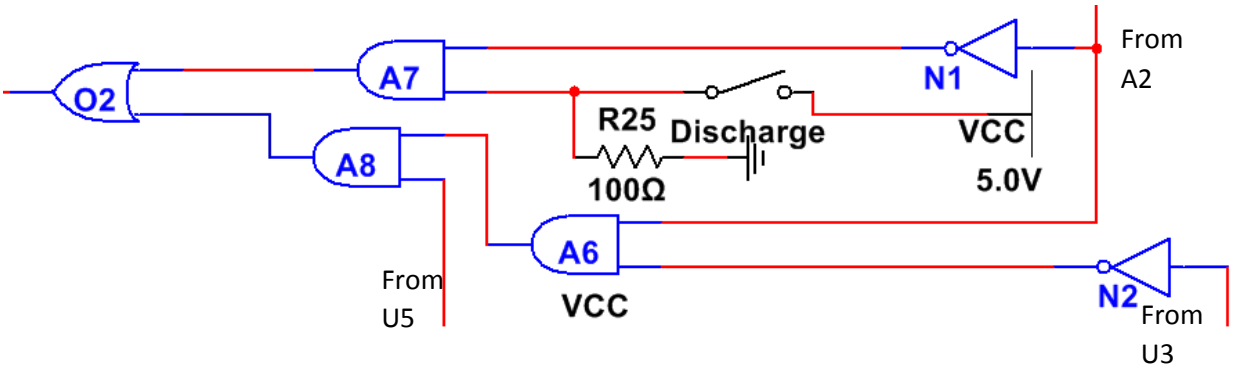


Figure 20: Final Logic for K2

Figure 20 illustrates the final logic controlling relay K2. N1 would take the inverse signal of A2 and send it to A7. If the Discharge switch was closed it would send 5V to A7 as well. O2 passed any 5V signal it saw onto K2 so if a test was not being run, i.e. A2 was low, Discharge could control K2. If a test was being run, A6 would take in the signal from A2 and the inverse signal of U3 from N2 and pass it on to A8. A8's other input was from the inverse output of the DFF U5, normally 5V. Once K2 had closed and reopened, U5's inverse output would go to 0V thus preventing K2 from reclosing.

A slight change was also made to the K3 control logic, using U5 that was added for K2, A4 was added that would allow K3 to close only after K2 had closed and reopened. This logic is shown in Figure 21.

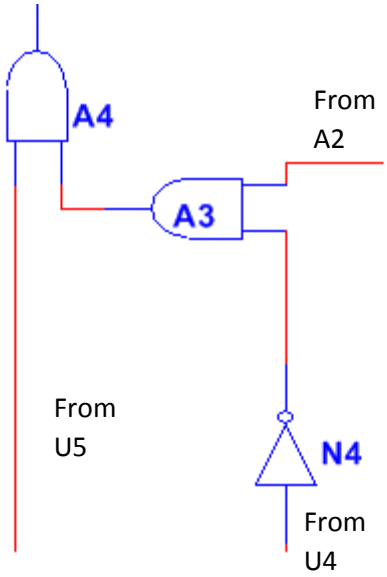


Figure 21: Final Logic for K3

Once these design modifications were made, and the theory proved via multiple smaller components, the rated components were purchased. A 10000µF capacitor with a voltage rating of 100V and maximum leakage of 20%, several differently rated resistors, the 5 relay units, (2 additional units were purchased in case of faulty operation or product), and pin sockets for chip/component mounting. A list detailing all components and items necessary for this project can be found in Appendix E.

The next step was the building of the coupling capacitor circuit itself. As the ordered 10000µF capacitor had not yet arrived, a work around was needed. The largest capacitors available were 220µF, so a bank of 45 of these capacitors was used. When the total capacitance of the bank was measured, it was exactly 10000µF.

After the circuit was built a test was initiated. Immediately it was noticed that the relays were not closing. Upon further inspection of the specifications it was discovered that the relays needed at least 62.5mA to operate. The initial design had the relays being powered from logic chips which couldn't output that much current. In order to address this issue and open collector (OC) AND gate, an NPN transistor and a diode were used to supply the power. The diode suppressed the fly back inductor current from the relay coil. An example of the circuit used to power each relay is shown in Figure 22.

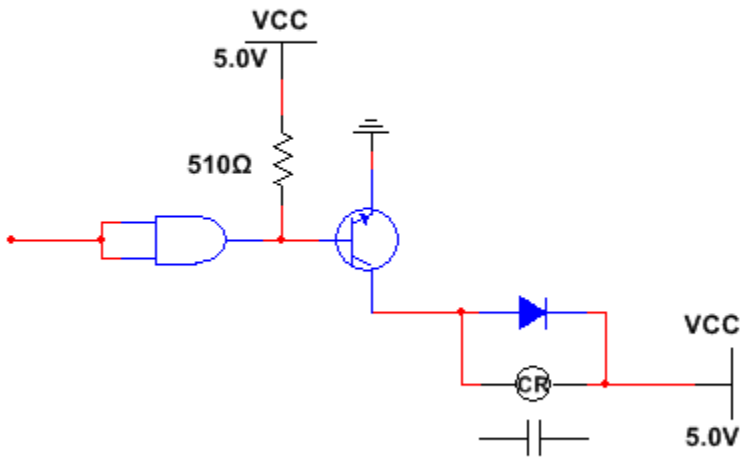


Figure 22: Circuit to Power Each Relay

Now that the relays were powered correctly another test was initiated with a 24V battery. During this test it was observed that the circuit reset whenever the IMB began to make a measurement. Three options for why this happened were: there was a glitch on the input signal from the IMB relays was resetting our circuit early, there was a problem with the logic that controlled the coupling capacitor relays, or the input SOS current from the IMB was causing the voltage over the capacitor to exceed 30V. The last option was discarded when another test was run and the voltage over the capacitor was monitored and never exceeded 30V.

The logic for controlling the relays was rebuilt three times and verified each time to determine that that was not the cause of the error. As for ruling out the glitch on the input signal from the IMB, an oscilloscope was set up to measure on a step input and the test was run again. It initially did not show a glitch on the signal. Eventually a test was run without the input from the IMB relays and the test ran through its states correctly and a spectrum was gathered. As time was becoming an issue, it was decided not to use the input from the IMB to reset the circuit and instead use a timer circuit that would reset the circuit about 20 seconds after the trigger had been sent to the IMB.

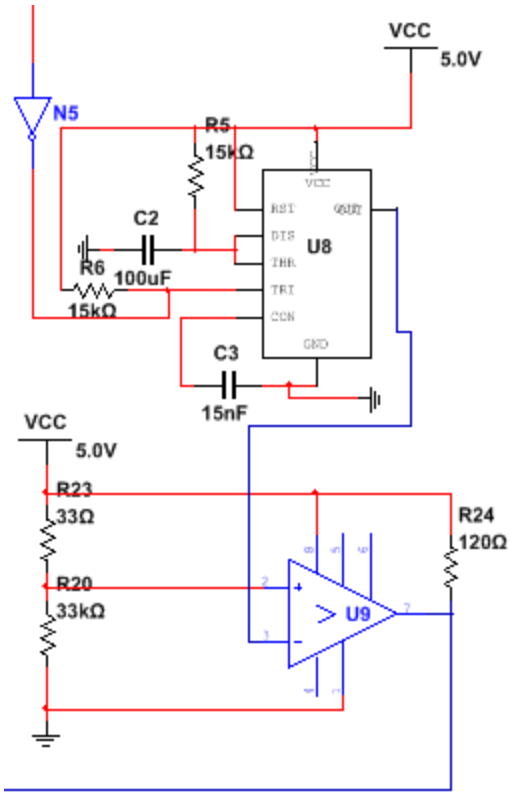


Figure 23: Timer Circuit to Reset System

The timer circuit begins timing the same time the trigger pulse is sent to the IMB. The 555 Timer (U8) along with the LM311 comparator (U9) initially outputs 5V. When the trigger initializes the timer, the output goes to 0V. After 20 seconds the value reasserts itself to 5V. The output is connected to a DFF positive edged clock input. This DFF resets the state machine and finishes the test. N5 is used to invert the trigger signal as this timer triggers on a negative edge.

With the circuit performing as designed another issue was discovered. The SOS current from the IMB was being cut off near the end of the test, which was corrupting our spectrum. A comparison of the spectrum without our circuit and with our circuit along with their respective SOS currents is shown in Figure 23.

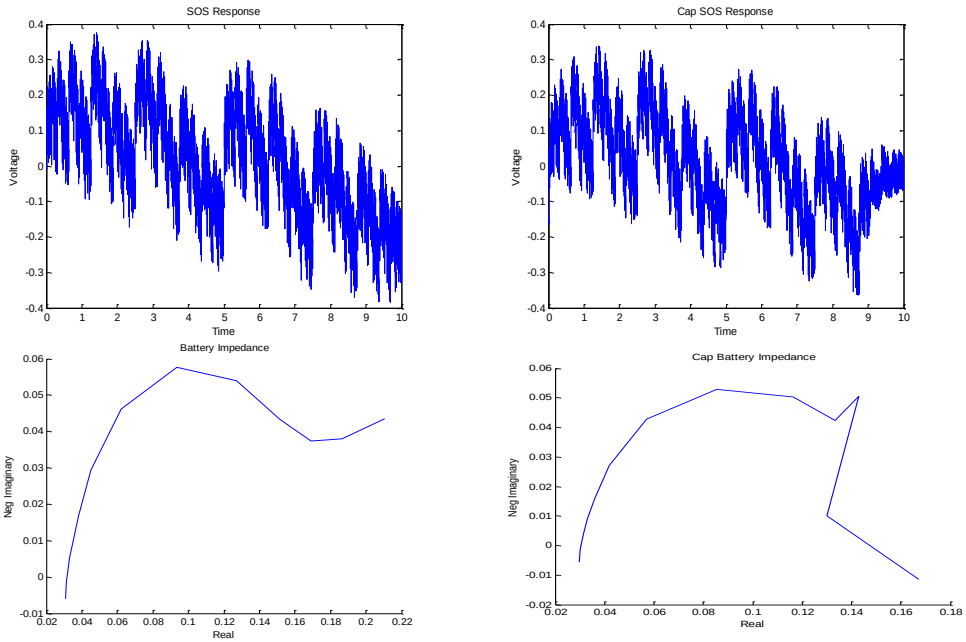


Figure 24: SOS and Spectrum with and without the Coupling Capacitor Circuit

As shown, in the beginning of the test the circuit performed correctly but near the end of the test the SOS current began to cut off. It was initially thought that the capacitors used in the capacitor bank was cutting this current off because they weren't rated to handle the voltage they were seeing, which was topping off at about 29V, with a 24V battery. Our mentor John Morrison had a different idea, he believed that the current drivers of the IMB were running out of compliance; most likely due to the fact that the capacitor bank being used was not exactly 0.01F. He then took our results from the coupling capacitor spectrum and cut off the corrupt data and recalculated the spectrum. This resulted in a much more accurate spectrum. This is shown in Figure 25.

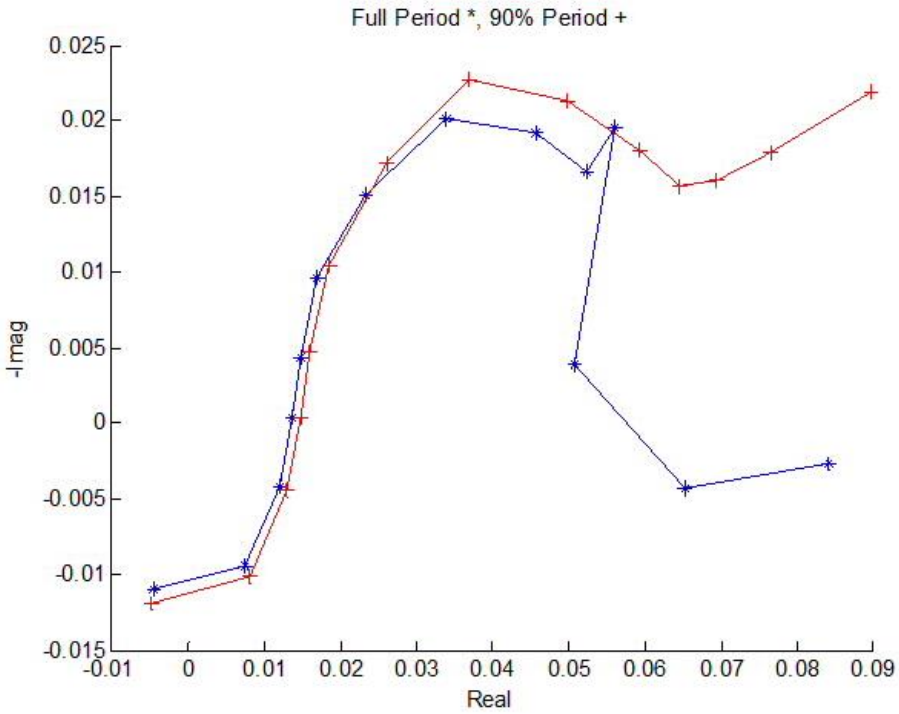


Figure 25: Normal and Recalculated Corrupt Spectrum

Now that the test had been correctly run and results gathered, it was time to begin designing the PCB, which would be our final deliverable. During the design the ordered 10000µF capacitor arrived and another test was run. This resulted in a much cleaner spectrum which matched the spectrum without the coupling capacitor circuit, shown in Figure 26.

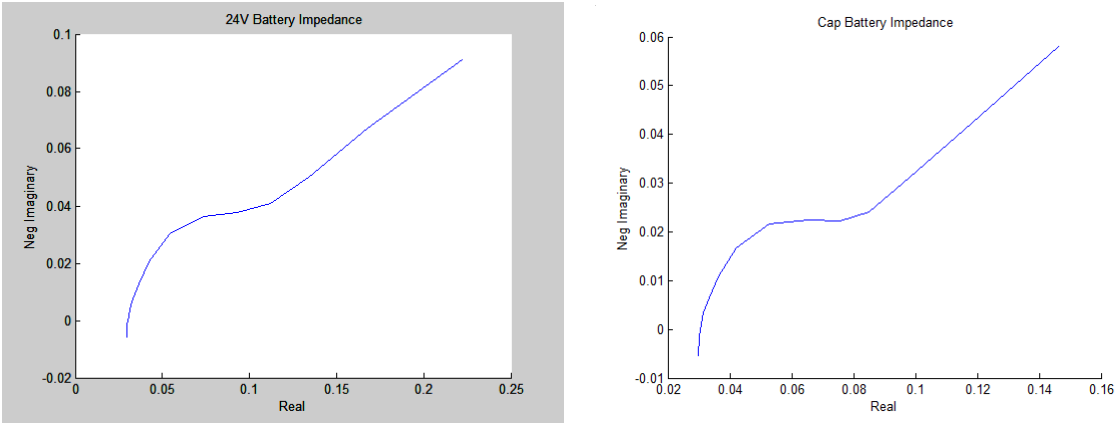


Figure 26: Spectra without Coupling Circuit (left), Spectra with Coupling Circuit and Correct Capacitor (right)

During the design of the PCB it was discovered that fitting the entire circuit onto one board would be triple the price of dividing the circuit into two pieces. So the first board would consist of the logic, which controlled the relays, as well as the relays themselves, and the second board would contain the coupling capacitor circuit, excluding the relays, the difference op-amp, the trigger pulse to the IMB, and the timer reset circuit. These designs are outlined in Figures 27 and 28.

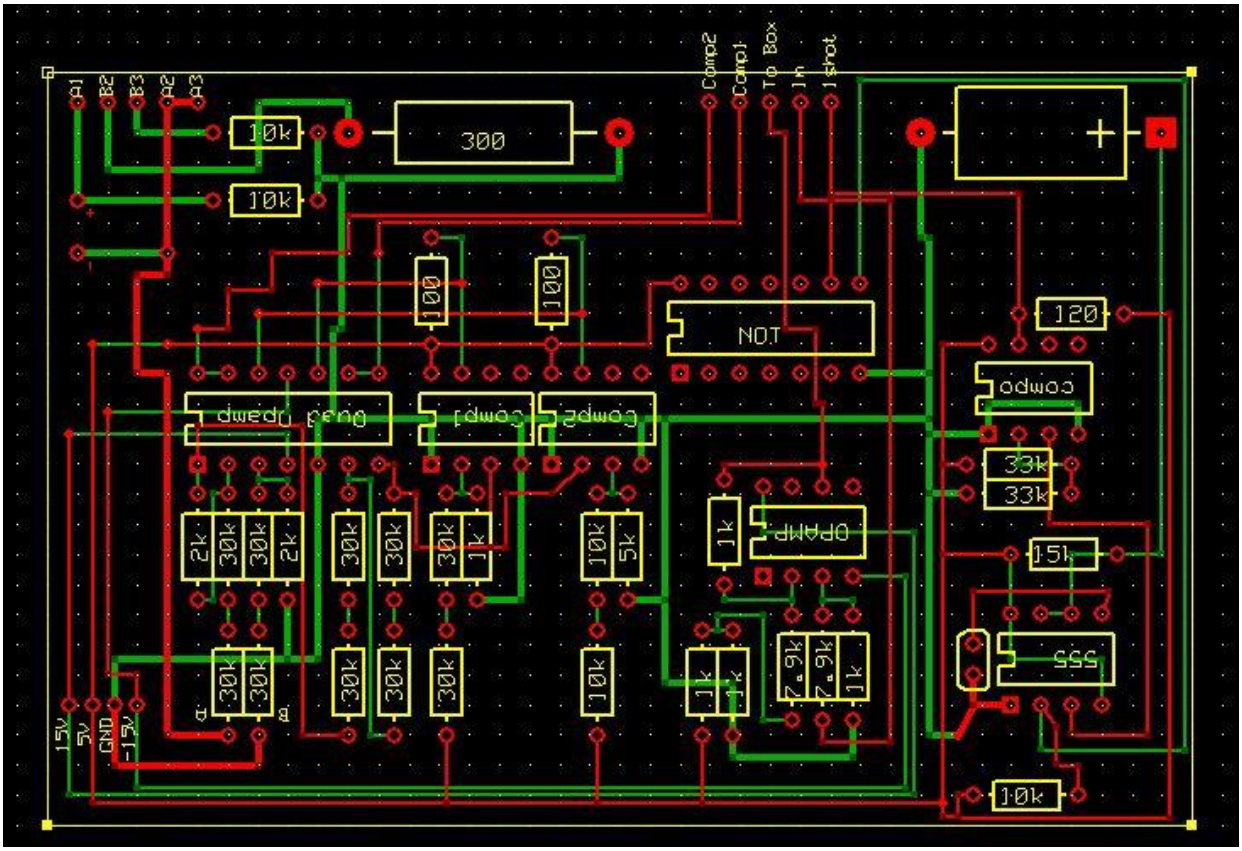


Figure 27: Comparator Circuit PCB

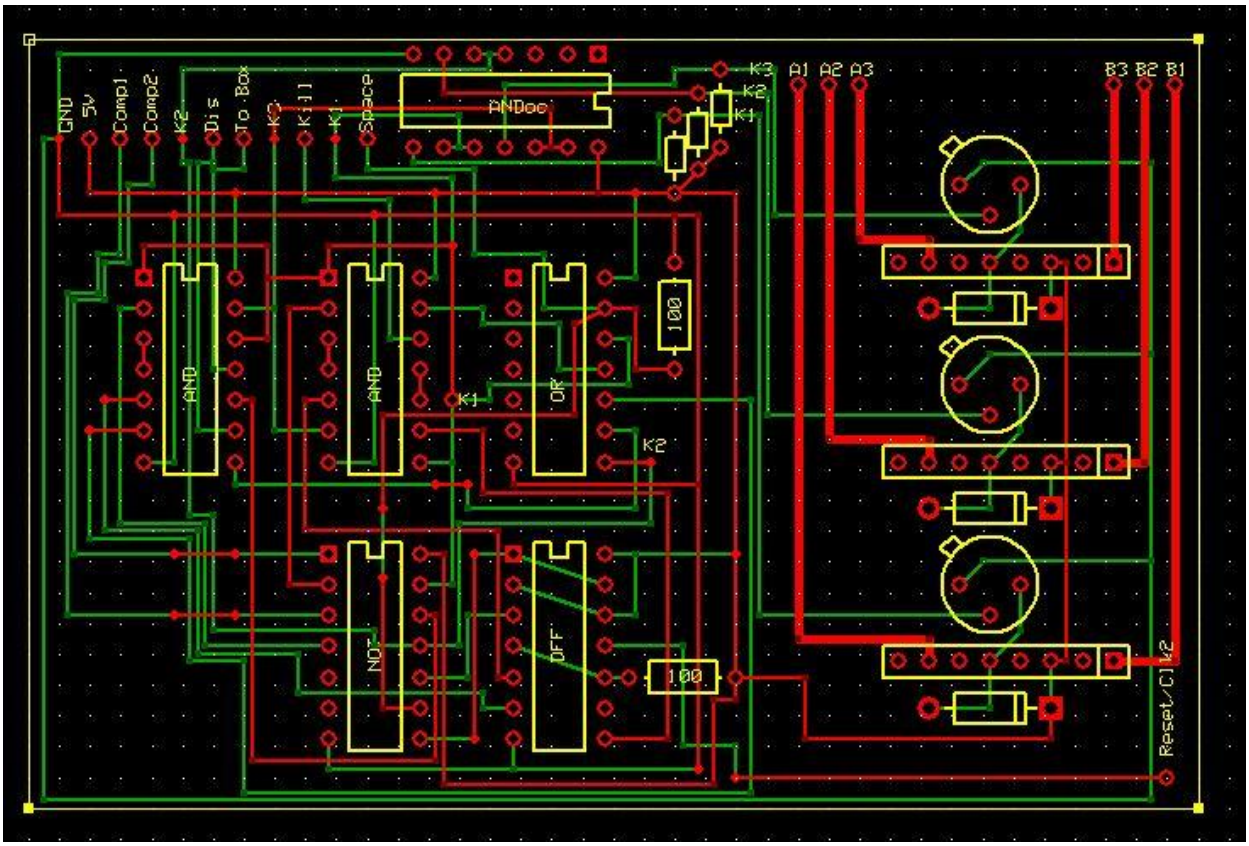


Figure 28: Logic Circuit PCB

With the PCB's designed and ordered a few more specific components needed to be ordered. A 300Ω resistor that could handle at least 1W for a few seconds was needed, two 10kΩ which would need to withstand half a watt, one normally opened (NO) pushbutton, and two switches. Also pin sockets for the chip components, digital logic, comparator op-amp, etc. were needed in case a chip was damaged or failed to operate correctly and needed replaced, as a damaged chip would ordinarily require it to be unsoldered. In addition the case that was to hold the final design, provided by Morrison, was metal so a non-conductive housing unit for each board was necessary. By using a 3-D printer, a holding case for each chip was developed, with openings to allow connections between the two was designed and manufactured.

When the PCB's and subsequent parts arrived, we began the assembly. All the parts were tested and connected via soldering to the PCBs. Once the PCB's were fully assembled they needed to be tested. The initial testing revealed several problems: an op-amp in the difference op-amp circuit was damaged and was outputting a wrong value, a second op-amp in the trigger portion of the circuit was powered incorrectly, the reset timer needed a pulse input and was receiving a steady state input so it could never time out, and the Kill_Switch and Discharge lacked pull down resistors.

1. The damaged op-amp was replaced;

2. The mistakenly powered pin (Pin 8) was a non-connection, so a solder bridge between it and the correct Pin 7 was created.
3. A break in the solder trace leading to the reset timer input was made and a filter with an RC time constant of 1ms was inserted.
4. Pull-down resistors were added to Kill_Switch and Discharge.

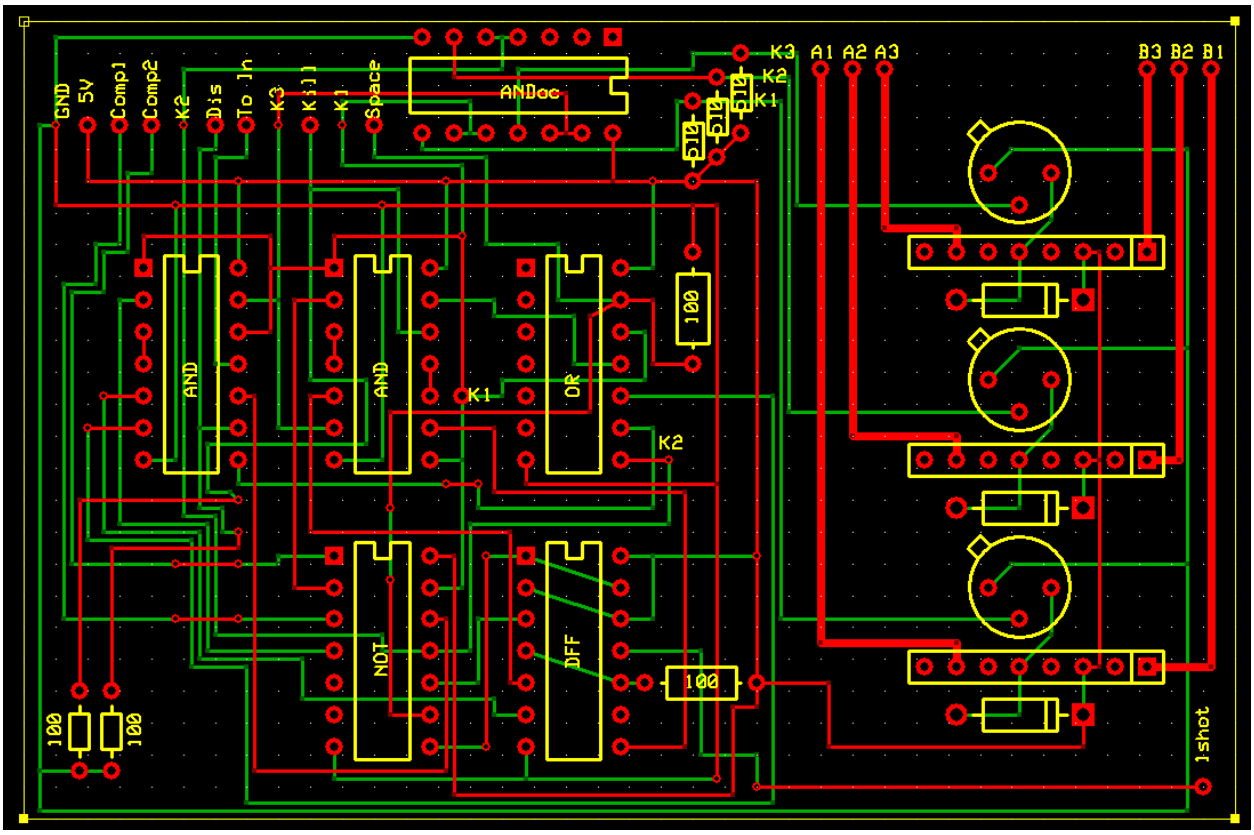


Figure 29: Updated Logic PCB With Pull-Down Resistors for Kill_Switch and Discharge (Bottom Left)

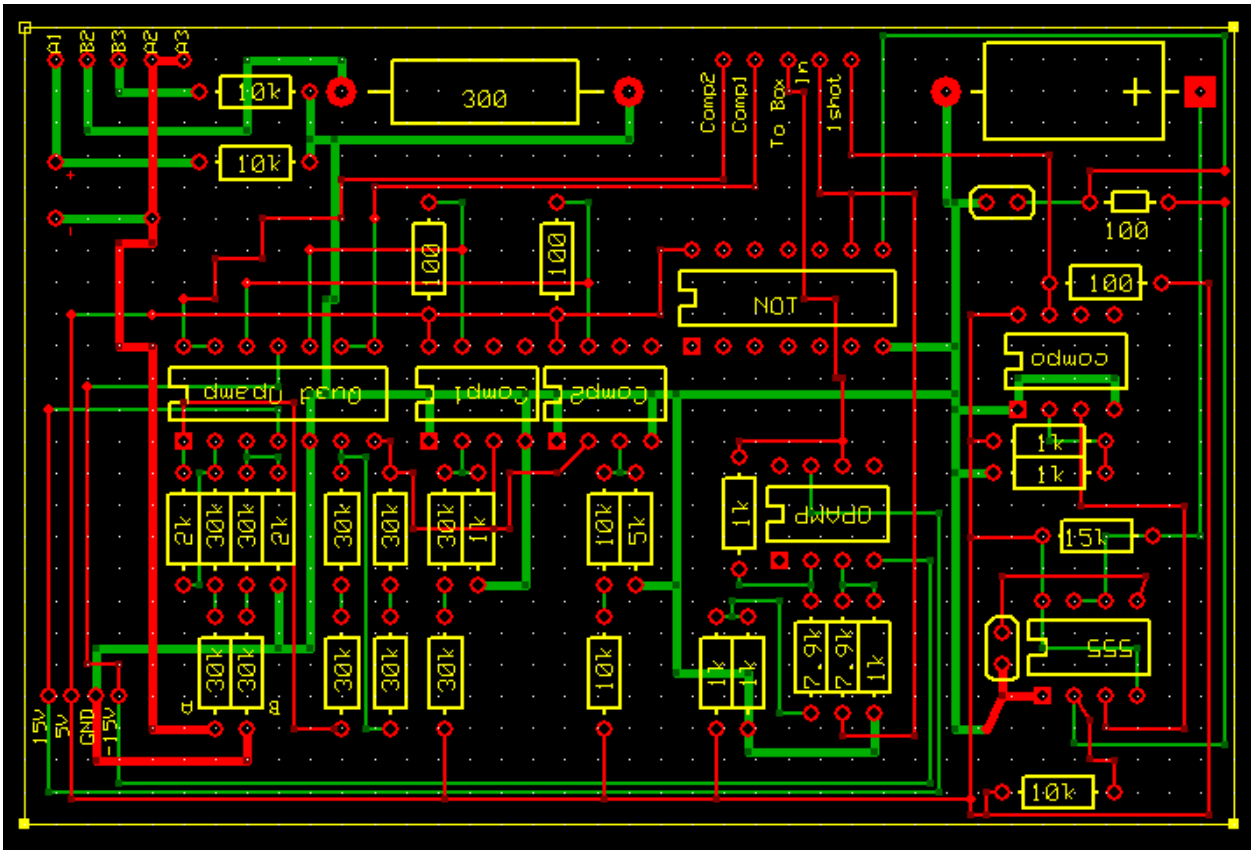


Figure 30: Updated Comparator Circuit PCB With RC Filter and Correctly Powered Op-Amp
(Top Right Below Large Capacitor, and Single Op-Amp Chip)

The final overall circuit schematic with the changes made is shown in Figure 31.

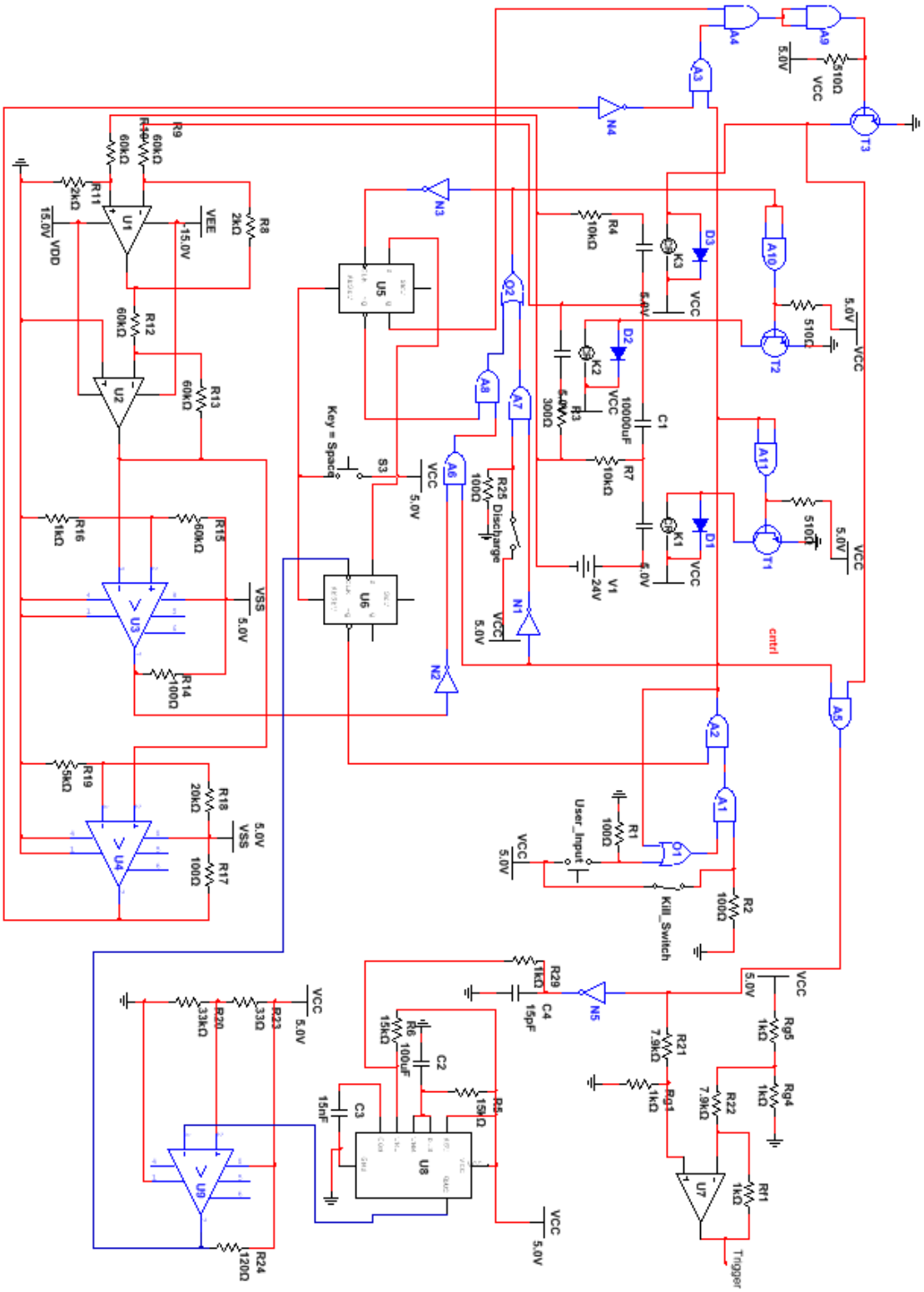


Figure 31:Final Overall Circuit Schematic

Following these modifications, permanent connections were made between the separate boards, as well as the switches and buttons. Once completed the PCBs and controls were installed in a case, and final testing was conducted to ensure operation, which produced an uncorrupted spectrum signifying the completion of the project.

Figure 32: Coupling Circuit (Front View)

Figure 33: Coupling Circuit (Rear View)

The testing methodology for running a full test using the Coupling Capacitor Circuit is outlined below.

Procedure for Hardware setup of IMB and CC

1. Place IMB on an uncluttered surface, plug power cable into IMB and plug into wall outlet
2. Place Coupling Circuit next to IMB
3. Place a power supply next to Coupling Circuit, plug power cable into power supply (Power supply must be rated for at least 1.5 watts)
4. Run separate leads from power supply to Coupling Circuit for +15V, -15V, +5V and Ground, respectively, taking care not to incorrectly power the system
5. Run the trigger lead from the IMB to Coupling Circuit, with the positive lead connecting to the "+Trig" input jack on the Coupling Circuit box, and the negative lead connecting to the "Gnd" input jack
6. Run the current leads from IMB to Coupling Circuit, with positive lead going to "Curr" input jack, and negative lead going to "Gnd"
7. Connect the battery in question to the Coupling Circuit with the positive terminal connected to "+Batt" input jack, and negative terminal to "Gnd"
8. Connect IMB to computer using USB interface cord

Procedure for Using the IMB and Coupling Circuit

1. Set up hardware as previously described
2. Open executable file: "Kane"*
3. Switch power on to Coupling Circuit and IMB respectively, switch "Kill" on Coupling Circuit to "On" (UP)
4. Confirm "Discharge" is off (Down)
5. Using "Kane", switch box on, via icon
6. Highlight calibration settings 139
7. Click "set"
8. Highlight "Measurement0"
9. Click "Limit runs"
    a. Select 1 run
10. Select "Trigger"
11. Enter -3 into Trigger value box
12. Enter 3.6 into Delta value box
13. Click "Run Sequence" (Purple play button)
14. Press "Start" on Coupling Circuit
15. Wait for a test to be completed
16. Flip "Discharge" on (UP)
17. Wait 20 seconds
18. Flip "Discharge" off (Down)
19. Either conduct another test starting at step 6, or move to step 20
20. Switch the IMB off via "Kane" power icon
21. Turn off power to both IMB and Coupling Circuit
22. Close "Kane"
23. Unhook hardware

Conclusion

This entire project had a lot of meaningful lessons to be taken from it. As a group we had to be diligent and manage our time wisely to meet our deadlines. We had to be creative to find solutions to the problems that kept cropping up. We had to make important decisions on what components to use and how we were going to implement them. And finally we had to make design sacrifices in order to move on and finish on time. This was primarily due to time conflictions with other classes.

There were several things we wish we could have fixed but ran out of time; one being the glitch on the IMB relay signal. During testing we attempted to use a low-pass RC filter to block the glitch from our circuit but couldn't get it to work. If we had more time we could have tested a different type of filter or a timing circuit to remove it before moving on and settling on the solution we did.

The mistakes we made with the PCB would have been removed. We would have like to make the changes we outlined earlier and reorder the PCB's but due to time and the cost we decided against it.

We would have liked to test our circuit against a larger battery than the 24V we had. Our final design had a max threshold of 100V due to limitations on the capacitor we could order. The scope of our project was to measure an uncorrupt spectrum through a coupling capacitor but we didn't have time to measure a battery larger than the 30V the IMB needed protection from.

All in all, this project was a huge success. We started out with an initial problem, how to build a circuit to allow the INL IMB test a large voltage battery. We ran simulations to prove it was possible and designed a system to do it. From that design we built, modified and built again a final circuit that is capable of blocking up to 100V while allowing the IMB to make a measurement.

Lessons Learned

- Time Management
    - Constantly racing the clock to meet a deadline due to unforeseen issues arising or other classes occupying our time.
    - Always leave time for errors
- Simulations do not always reflect reality
    - Our simulations did not always account for our components specifications, (example, the relays needed more current to operate then the logic chips could handle.)
- The solution to the glitch on the IMB relay signal was a temporary fix.
    - In a job situation our work around would not be an acceptable fix to the problem as one of the design constraints of this project was to use the IMB relay signal.

Appendix A

Test Cell Voltage Derivation

```
        Constants from circuit
Rcs=20000;
Rl=90000;
Rc=0.9;
Rs=10000;
R1=0.015;
R2=0.015;
R3=0.020;
C=0.01;
Ct=9;
        Chosen constants to simplify calculations
fo=40e3;
deltaT=fo^-1;
tstop=0.0125^-1;
time=(0:deltaT:tstop);
t1=Rc*Rl/(Rc+Rl);
t2=1/(C*Rc);
t3=1/(C*(Rc+Rl));
t4=Rs*R2*R3+R1*Rs*(R2+R3);
t5=R2*R3+(R2+R3)*(R1+Rs);
t6=Rs*(R1+R3)/(Ct*t4);
t7=(R1+R3+Rs)/(Ct*t5);
t8=t4/t5;
a1=Rcs+t1+t8;
a2=Rcs*(t3+t7)+t1*(t2+t7)+t8*(t3+t6);
a3=Rcs*t3*t7+t1*t2*t7+t3*t6*t8;
a4=t8/a1;
a5=t3+t6;
a6=t3*t6;
a7=a2/a1;
a8=a3/a1;
        Calculating test cell voltage
vin=ones(length(time),1);
vout=zeros(length(time),1);
x=zeros(length(time),1);
for n=1:length(time);
        x(n+2)=vin(n)-x(n+1)*(deltaT*a7-2)-x(n)*(deltaT^2*a8+1-deltaT*a7);
        vout(n)=a4*(vin(n)+x(n+1)*deltaT*(a5-a7)+x(n)*(deltaT^2*(a6-a8)-deltaT*(a5-a7)));
end
                        %Vout is the test cell voltage
```

Capacitor and Source Voltage Derivations

Constants from circuit

```
Cs=.01;
Rcs=20000;
Rs=10000;
Rlk=90000;
ESR=.9;
R1=15e-3;
R2=15e-3;
R3=20e-3;
C1=9;
```

Chosen constants to simplify calculations

```
Tau1=Cs*ESR;
Tau2=Cs*(ESR+Rlk);
Tau3=C1*R2;
Tau4=C1*(R2+R3);
Tau5=(Tau3*R3+Tau4*(R1+Rs))/(R1+R3+Rs);
Tau6=(Tau3*R3+Tau4*R1)/(R1+R3);
K1=Rcs*Rs*(R1+R3)*Tau2*Tau6/(Tau1*Tau5*(R1+R3+Rs)*Rlk+Tau2*Tau6*(R1+R3)*Rs+Tau2*Tau5*(R1+R3
+Rs)*Rcs);
K2=(Tau2+Tau6)/(Tau2*Tau6);
K3=1/(Tau2*Tau6);
K6=Rcs*(Tau1*Tau5*Rlk*(R1+R3+Rs)+Tau2*Tau6*(R1+R3)*Rs)/(Tau1*Tau5*(R1+R3+Rs)*Rlk+Tau2*Tau6*(
R1+R3)*Rs+Tau2*Tau5*(R1+R3+Rs)*Rcs);
K7=((Tau1+Tau5)*(R1+R3+Rs)*Rlk+(Tau2+Tau6)*(R1+R3)*Rs)/(Tau1*Tau5*(R1+R3+Rs)*Rlk+Tau2*Tau6*(R
1+R3)*Rs);
K8=((R1+R3+Rs)*Rlk+(R1+R3)*Rs)/(Tau1*Tau5*(R1+R3+Rs)*Rlk+Tau2*Tau6*(R1+R3)*Rs);
K9=((Tau1+Tau5)*(R1+R3+Rs)*Rlk+(Tau2+Tau6)*(R1+R3)*Rs+(Tau2+Tau5)*(R1+R3+Rs)*Rcs)/(Tau1*Tau5*(
R1+R3+Rs)*Rlk+Tau2*Tau6*(R1+R3)*Rs+Tau2*Tau5*(R1+R3+Rs)*Rcs);
K10=((R1+R3+Rs)*Rlk+(R1+R3)*Rs+(R1+R3+Rs)*Rcs)/(Tau1*Tau5*(R1+R3+Rs)*Rlk+Tau2*Tau6*(R1+R3)*R
s+Tau2*Tau5*(R1+R3+Rs)*Rcs);
K4=K9;
K5=K10;
```

```
        Calculating current source voltage and capacitor voltage
Ka=K6;
Kb=K7;
Kc=K8;
Kd=K9;
Ke=K10;
Vx=zeros(1,N+NN);
Y1=zeros(1,N+NN);
Y2=zeros(1,N+NN);
A=[0,1;-(1+Ke*dt^2-Kd*dt),-(dt*Kd-2)];
B=[0;1];
C=Ka*[((Kc-Ke)*dt^2-(Kb-Kd)*dt),(Kb-Kd)*dt];
Vin=Iin*Ka;                              %Where Iin is a SOS signal
for i=2:N+NN                             %Where N+NN is the number of points of the time signal
        X=A*[Y1(i-1);Y2(i-1)]+B*Iin(i-1);
        Vx(i)=C*X;
        Y1(i)=X(1);
        Y2(i)=X(2);
end
Vin=Vin+Vx;
Vcs=Vin;                                 %Current Source Voltage
Vcap=ones(1,N+NN)*Vb;           %Where Vb=300
Vcap=Vcap-Vcs;                  %Capacitor Voltage
```

Code used for voltage response of test cell

```
%Andrew Storro & Mark Clagett
%Derivation of Computer Simulation Model
% clear all;
close all; clc
%Constants
Rcs=20000;
Rl=90000;
Rc=0.9;
Rs=10000;
R1=0.015;
R2=0.015;
R3=0.020;
C=0.01;
Ct=9;
s=tf('s');
Isos=0;

%frequency constants
fo=40e3;
deltaT=fo^-1;
tstop=0.0125^-1;
time=(0:deltaT:tstop);
freq=zeros(18,1);
w=zeros(18,1);
for k= 1:18;
   freq(k)=0.0125*2^(k-1);
   w(k)=2*pi*freq(k);
end

%calculated constants
t1=Rc*Rl/(Rc+Rl);
t2=1/(C*Rc);
t3=1/(C*(Rc+Rl));
t4=Rs*R2*R3+R1*Rs*(R2+R3);
t5=R2*R3+(R2+R3)*(R1+Rs);
t6=Rs*(R1+R3)/(Ct*t4);
t7=(R1+R3+Rs)/(Ct*t5);
t8=t4/t5;

a1=Rcs+t1+t8;
a2=Rcs*(t3+t7)+t1*(t2+t7)+t8*(t3+t6);
a3=Rcs*t3*t7+t1*t2*t7+t3*t6*t8;
a4=t8/a1;
a5=t3+t6;
a6=t3*t6;
a7=a2/a1;
a8=a3/a1;

%initial conditions
vin=ones(length(time),1);
vout=zeros(length(time),1);
x=zeros(length(time),1);
```

```
%state variable recursive model
for n=1:length(time);

   x(n+2)=vin(n)-x(n+1)*(deltaT*a7-2)-x(n)*(deltaT^2*a8+1-deltaT*a7);
   vout(n)=a4*(vin(n)+x(n+1)*deltaT*(a5-a7)+x(n)*(deltaT^2*(a6-a8)-deltaT*(a5-a7)));
end
figure(1)

%plot of step input
plot(time,vout,'Linewidth',3);
title('Step Response');
xlabel('Time');
ylabel('Voltage');
hold on
num=[a4 a4*a5 a4*a6];
den=[1 a7 a8];
hz=tf(num,den);
stepresp=step(hz,time);
plot(time,stepresp,'r','Linewidth',2);
plot(abc(:,1),abc(:,2),'g')
legend('Recursive','Calculated','Multisim');
Iin=0;

%sum of sines input
for k=1:18;
   Iin=Iin+sin(2*pi*0.0125*2^(k-1).*time);
end
vout=zeros(length(time),1);
x=zeros(length(time),1);
for n=1:length(time);
    x(n+2)=Iin(n)-x(n+1)*(deltaT*a7-2)-x(n)*(deltaT^2*a8+1-deltaT*a7);
   vout(n)=a4*Rcs*(Iin(n)+x(n+1)*deltaT*(a5-a7)+x(n)*(deltaT^2*(a6-a8)-deltaT*(a5-a7)));
end
%plot of sum of sines input
figure(2)
subplot(2,1,1);
plot(time,vout);
title('Sum of Sines Response');
xlabel('Time');
ylabel('Voltage');
subplot(2,1,2);
plot(time,Iin,'r');
title('Sum of Sines');
xlabel('Time');
ylabel('Current');

%nyquist calculations
num=[t8 t8*t6];
den=[1 t7];
respHz=zeros(18,1);
for k=1:18;
    omega=1*j*w(k);
    respHz(k)=(num(1)*omega+num(2))/(den(1)*omega+den(2));
```

```
end
reel=zeros(18,1);
imagine=zeros(18,1);

for m=1:18;
   for k=2:length(time)-1;
       reel(m)=reel(m)+sin(w(m)*k*deltaT)*vout(k+1);
       imagine(m)=imagine(m)+cos(w(m)*k*deltaT)*vout(k+1);
   end
   reel(m)=2*reel(m)/length(time);
   imagine(m)=2*imagine(m)/length(time);
end
 %nyquist plot
figure(3)
plot(real(respHz),-imag(respHz),'b-o',reel,-imagine,'r-x');
title('Impedance Nyquist');
legend('Calculated','Recursive');
xlabel('Real Part');
ylabel('Negative Imaginary Part');
grid
```

Appendix C

Code used for calculating capacitor voltage and source voltage

```
%%%%% 300V HCSD System Simulation%%%%%%%%%
%%%%%%%%%%% It Works %%%%%%%%%%%%%%%%%%%%
% Does P periods backwards in time and one period forward in time part (1-fract) of this is thrown away
% Flips frequencies to help transient response, -1: flip +1: no flip
flip=1;% not used
% reduced time works best if kept octave harmonic
RMS=.25;
M=15; % number of frequencies at m=15 octave harmonic
Peak=RMS*(2/M)^.5;
P=.1; % number of backward periods
fstart= .1; % start frequency

Vb=300;
alp=2;
for i=1:M
 f(i)=fstart*(alp)^(i-1);% The 2^step gives the frequency step
end

fs=40e3;%16*fend; % sample frequency for dt step
dt=fs^-1; % time step
N=ceil(fs/fstart) % Number of time steps in the first period

NN=ceil(P*N); % points of backward time signal

%%%% Build the SOS %%%%%%
timeArray = (-NN:(N-1))*dt;
sosSignal = zeros(size(timeArray));
for i = 1:M
        sosSignal = sosSignal + (Peak*(flip)^i*sin(2*pi*f(i).*timeArray));
end
Iin=sosSignal;
ts=zeros(1,N+NN);
for i=1:N+NN
 ts(i)=(i-1)*dt;
end

%%%%%%%%%%% Recursive 300V %%%%%%%%%%%%%%
Cs=.01;
Rcs=20000;
Rs=10000;
Rlk=90000;
ESR=.9;
%%%% Test Cell #3 %%%%%%%%%%
R1=15e-3;
R2=15e-3;
R3=20e-3;
C1=9;
%%%% Recursive Constants %%%%%%%%%%
Tau1=Cs*ESR;
Tau2=Cs*(ESR+Rlk);
Tau3=C1*R2;
Tau4=C1*(R2+R3);
```

```
Tau5=(Tau3*R3+Tau4*(R1+Rs))/(R1+R3+Rs);
Tau6=(Tau3*R3+Tau4*R1)/(R1+R3);
Check=[dt Tau1 Tau2 Tau3 Tau4 Tau5 Tau6];

K1=Rcs*Rs*(R1+R3)*Tau2*Tau6/(Tau1*Tau5*(R1+R3+Rs)*Rlk+Tau2*Tau6*(R1+R3)*Rs+Tau2*Tau5*(R1+R3
+Rs)*Rcs);

K2=(Tau2+Tau6)/(Tau2*Tau6);

K3=1/(Tau2*Tau6);

K6=Rcs*(Tau1*Tau5*Rlk*(R1+R3+Rs)+Tau2*Tau6*(R1+R3)*Rs)/(Tau1*Tau5*(R1+R3+Rs)*Rlk+Tau2*Tau6*(
R1+R3)*Rs+Tau2*Tau5*(R1+R3+Rs)*Rcs);

K7=((Tau1+Tau5)*(R1+R3+Rs)*Rlk+(Tau2+Tau6)*(R1+R3)*Rs)/(Tau1*Tau5*(R1+R3+Rs)*Rlk+Tau2*Tau6*(R
1+R3)*Rs);

K8=((R1+R3+Rs)*Rlk+(R1+R3)*Rs)/(Tau1*Tau5*(R1+R3+Rs)*Rlk+Tau2*Tau6*(R1+R3)*Rs);

K9=((Tau1+Tau5)*(R1+R3+Rs)*Rlk+(Tau2+Tau6)*(R1+R3)*Rs+(Tau2+Tau5)*(R1+R3+Rs)*Rcs)/(Tau1*Tau5*(
R1+R3+Rs)*Rlk+Tau2*Tau6*(R1+R3)*Rs+Tau2*Tau5*(R1+R3+Rs)*Rcs);
K10=((R1+R3+Rs)*Rlk+(R1+R3)*Rs+(R1+R3+Rs)*Rcs)/(Tau1*Tau5*(R1+R3+Rs)*Rlk+Tau2*Tau6*(R1+R3)*R
s+Tau2*Tau5*(R1+R3+Rs)*Rcs);
K4=K9;
K5=K10;
Vcs=zeros(1,N+NN);
Vtc=zeros(1,N+NN);
Ka=K1;
Kb=K2;
Kc=K3;
Kd=K4;
Ke=K5;
Vx=zeros(1,N+NN);
Y1=zeros(1,N+NN);
Y2=zeros(1,N+NN);
A=[0,1;-(1+Ke*dt^2-Kd*dt),-(dt*Kd-2)];
B=[0;1];
C=Ka*[((Kc-Ke)*dt^2-(Kb-Kd)*dt),(Kb-Kd)*dt];

Vin=Iin*Ka;
for i=2:N+NN
 X=A*[Y1(i-1);Y2(i-1)]+B*Iin(i-1);
 Vx(i)=C*X;
 Y1(i)=X(1);
 Y2(i)=X(2);
end
Vin=Vin+Vx;
Vtc=Vin;

Ka=K6;
Kb=K7;
Kc=K8;
Kd=K9;
```

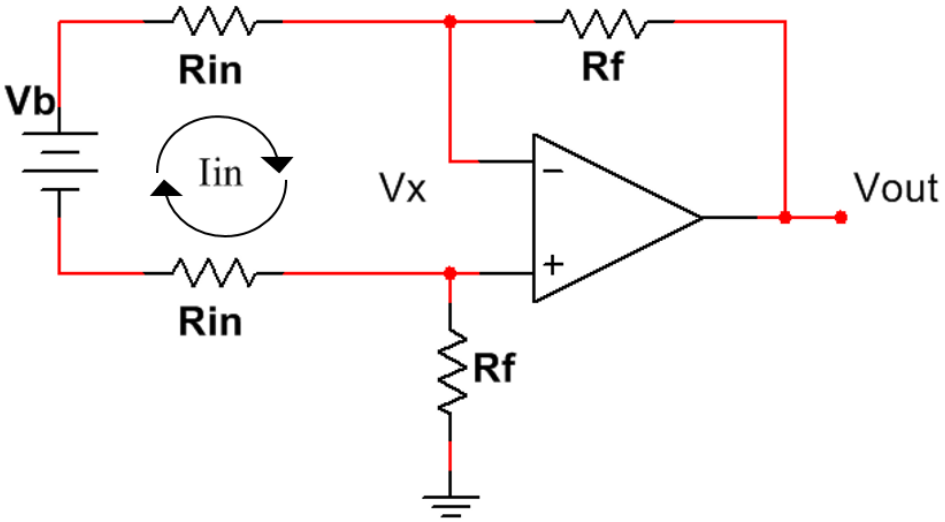
```
Ke=K10;

Vx=zeros(1,N+NN);
Y1=zeros(1,N+NN);
Y2=zeros(1,N+NN);
A=[0,1;-(1+Ke*dt^2-Kd*dt),-(dt*Kd-2)];
B=[0;1];
C=Ka*[((Kc-Ke)*dt^2-(Kb-Kd)*dt),(Kb-Kd)*dt];


Vin=Iin*Ka;
for i=2:N+NN
 X=A*[Y1(i-1);Y2(i-1)]+B*Iin(i-1);
 Vx(i)=C*X;
 Y1(i)=X(1);
 Y2(i)=X(2);
end
Vin=Vin+Vx;
Vcs=Vin;

V=zeros(1,N);
for i=1:N
 V(i)=Vtc(NN+i)/Peak;
end

ii=1;

% Code for conventional syncronous detection of each component
% This will be used to obtain compensation error
for j=1:M
 sum=0;
 ssum=0;
 for i=1:N

  t=(i-1)*dt;
  % for synchronous detection ssum gets the "In phase"
  % and sum gets the "Quadrature phase"
  ssum=ssum+V(i)*sin(2*pi*f(j)*(t));
  sum=sum+V(i)*cos(2*pi*f(j)*(t));
 end
 VsD=ssum/(.5*N); % (N) is the record length
 VcD=sum/(.5*N); % (N) as above
 Vs(j)=VsD; % In phase component
 Vc(j)=VcD; % Quadurature component
 disp(num2str(j)) % progress
end

%%%%%%%%%% Compute Ideal Response %%%%%%%%%%%%%%%%%%%%

for i=1:M
 s=2*pi*f(i);
 Z(i)=R1+(R3+s^2*C1^2*R3*R2*(R3+R2))/(1+s^2*C1^2*(R3+R2)^2)-
1j*(s*C1*R3^2)/(1+s^2*C1^2*(R3+R2)^2);
 MH(i)=abs(Z(i));
 RH(i)=real(Z(i));
```

```
 IH(i)=imag(Z(i));
 PHI(i)=atan(IH(i)/RH(i))*180/pi;
end
for i=1:M
 VVVd(i)=(Vs(i)^2+Vc(i)^2)^.5; % Magnitude of each detected component
 Ph(i)=atan2(Vc(i), Vs(i))*180/pi;
end
Vcap=ones(1,N+NN)*Vb;
Vcap=Vcap-Vcs;
figure(ii)
hold on
plot(ts,Vcs)
title('Current Source Voltage')
xlabel('Time')
ylabel('Volts')
hold off
ii=ii+1
figure(ii)
hold on
plot(ts,Vcap)
title('Cap Voltage')
xlabel('Time')
ylabel('Volts')
hold off
ii=ii+1;
figure(ii)
hold on
plot(log10(f), VVVd,'*-', log10(f), MH, 'o-')
%axis([-2 1 -3e-3 50e-3])
title('TC3 Responce, HCSD *, Ideal o')

xlabel('Log Frequency')
ylabel('Imped Mag')
hold off

%% Phase Results plots
ii=ii+1;
figure(ii)
hold on
plot(log10(f), Ph, '*-', log10(f), PHI, 'o-')
%axis([-2 1 -25 0])
title('TC3 Phase, HCSD *, Ideal o')
xlabel('Log Frequency')
ylabel('Phase')
hold off
%%%% Nyquist plots
ii=ii+1;
figure(ii)
hold on
plot(Vs, -Vc, '*-', RH, -IH, 'o-') % The INL convention is negative imaginary
%axis([.0125, .0155, -4e-4, 14e-4])
title('TC3 Nyquist, HCSD *, Ideal o')
xlabel('Real')
ylabel('Complex')
```

hold off

Appendix D

Validation of gain chosen for difference op-amp to ensure safety



1. $Vb = 2 * Rin * Iin$
2. $Iin = \frac{(0-Vx)}{Rf}$
3. $\frac{Vb}{2*Rin} = Iin$
4. $\frac{Vb}{2*Rin} = \frac{-Vx}{Rf}$
5. $\frac{-Rf*Vb}{2*Rin} = Vx$

Rf=1kΩ, Rin=30kΩ, Vb=300V

A. $\frac{-Rf*Vb}{2Rin} = Vx$

B. $\frac{-1k\Omega*300V}{2*30k\Omega} = -5V$

C. Vx= -5V

Parts List

- 1x 10000uF capacitor
    - 100V rating
    - 20% leakage
    - Aluminum housing
- 1x 220uF capacitor
- 2x 15pf capacitor
- 3x 2N2219A NPN Transistors
- 1x 300 Ω resistor 2W rating
- 3x 510 Ω
- 1x 5k Ω
- 8x 100 Ω
- 5x 10k Ω resistor 1W rating
- 7x 1k Ω resistor
- 2 x 7.9k Ω resistor
- 10x 30k Ω 1W rating
- 2x 2k Ω resistor
- 1x 15k resistor
- 3x 1N0049 diodes
- 1x 7432
- 1x 7474
- 1x 7409
- 2x 7404
- 2x 7408
- 1x LM 148
- 3x LM311
- 1x UA741
- 1x LM555
- 3x 8-SIP
- 8x 16-DIP
- 5x 8-DIP
- 1x NO Pushbutton
- 2x SPST switches
- 1x Control Logic PCB
- 1x Comparator PCB

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